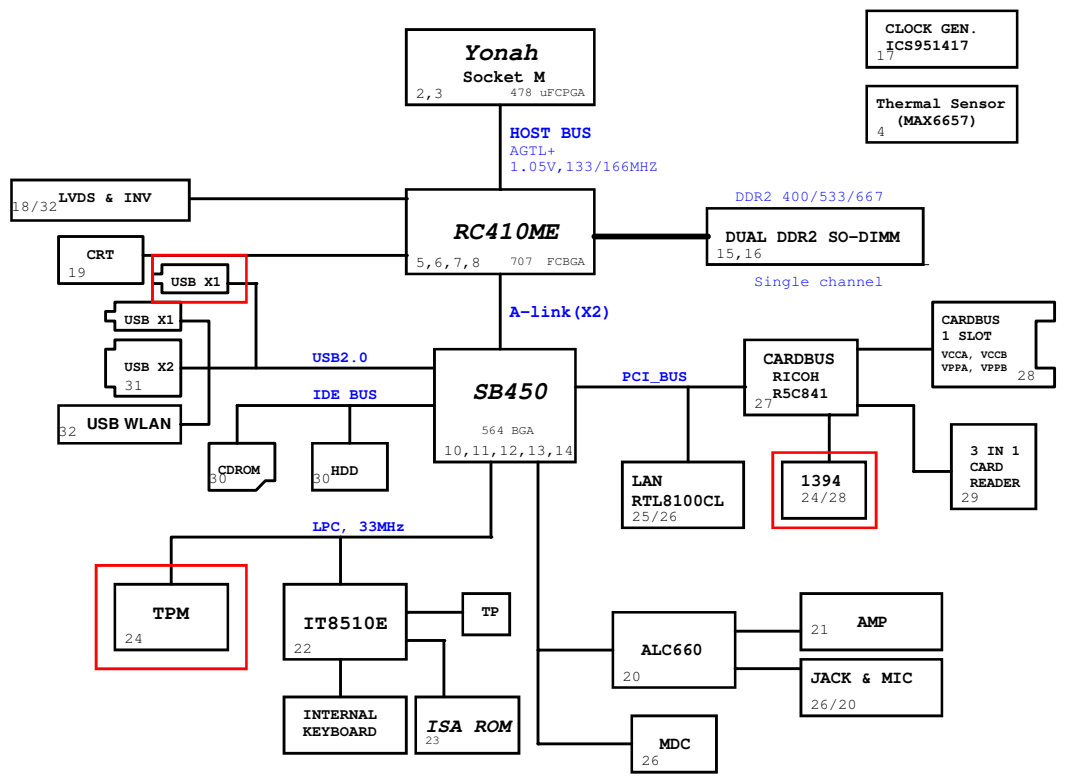


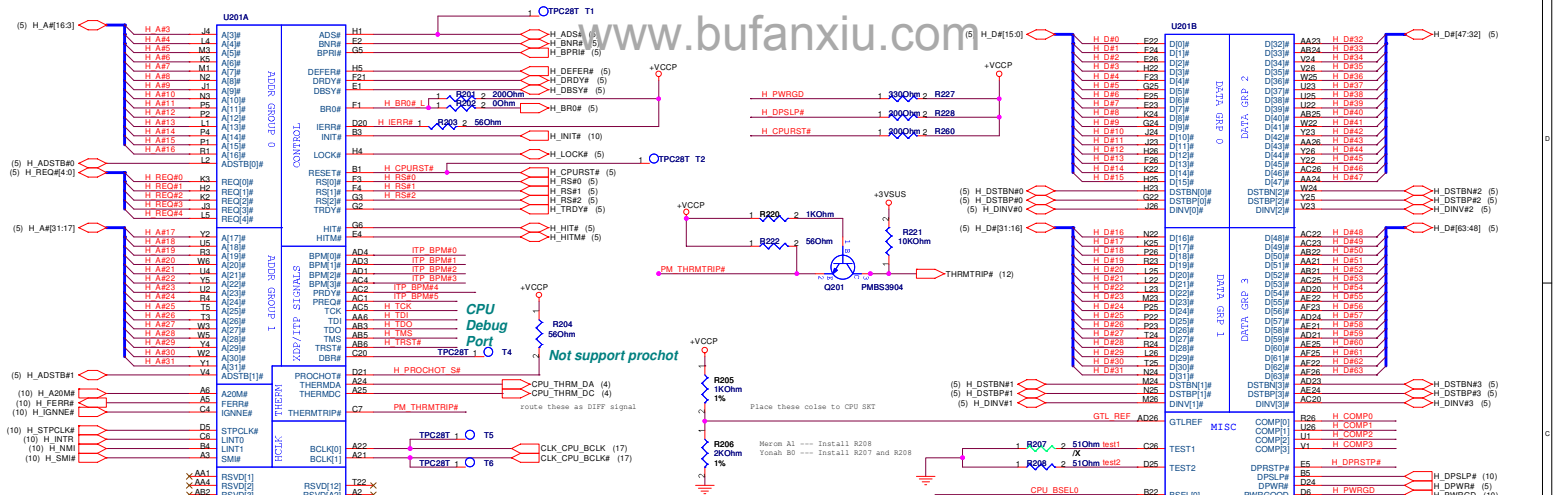
Yonah/RC410ME/IXP450 BLOCK DIAGRAM

PAGE	TITLE
01	Block Diagram
02	Yonah CPU(1)
03	Yonah CPU(2)
04	THERMAL SENSOR/FAN
05	RC410ME AGTL+ I/F (1)
06	RC410ME A-LINK (2)
07	RC410ME DDR2 I/F (3)
08	RC410ME VIDEO I/F (4)
09	RC410ME POWER (5)
10	SB450 ALINK/PCI/CPU/LPC (1)
11	SB450 IDE (2)
12	SB450 AC97/USB (3)
13	SB450 POWER (4)
14	SB450 STRAPS (5)
15	DDR2 DIMMs
16	DDR2 TERMINATION
17	CLOCK GEN.-ICS951417
18	LVDS
19	CRT
20	ALC660/MIC
21	AMP/Speaker
22	EC IT8510E
23	ISA ROM
24	1394/TPM
25	LAN 8100CL
26	RJ11+45 & MDC
27	CARDBUS R5C841
28	PCMCIA&Debug Port
29	SD/MS
30	HDD/CD-ROM
31	USB/LED/TP
32	INV/WLAN
33	Hole
34	System poweron sequency
35	System Resource
61	Power-SEQUENCE
62	Power-VCORE
63	Power-3VSUS/5VSUS
64	Power-1.8VSUS/1.2VS
65	Power-VCCP/1.5VS/0.9VS
66	Power-BAT
67	Power-CHARGE
68	Power-POWER LIMIT/AC-BAT DETECT
69	Power-LOAD SWITCH
70	Power Block Diagram
**	
**	



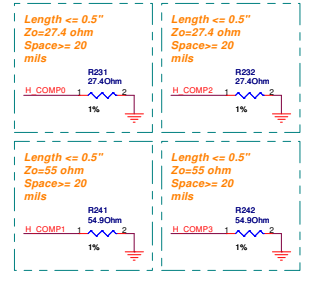
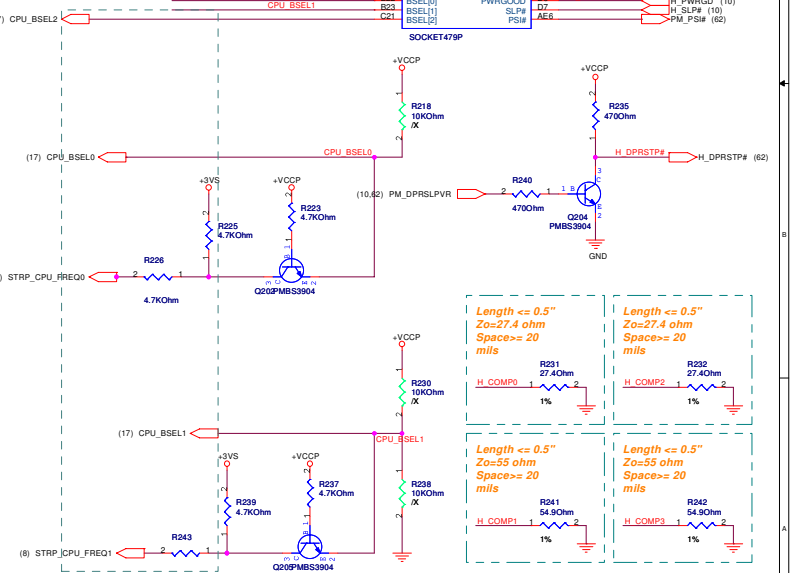
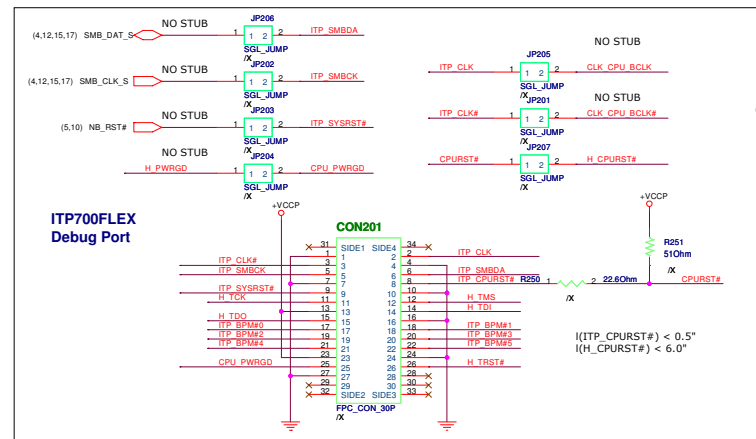
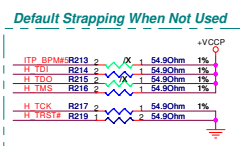
ASUS		Title : BLOCK DIAGRAM	
ASUS-IB Server	Engineer:	shelleys	
Size	Project Name	Rev	
Custom	T19R	1.0	
Date: 11/20/2008	Sheet	1 of 45	

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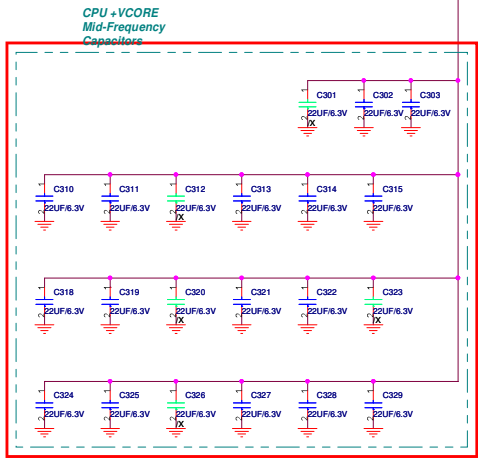
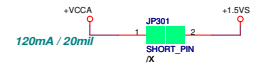
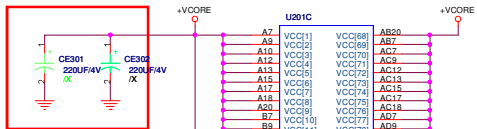
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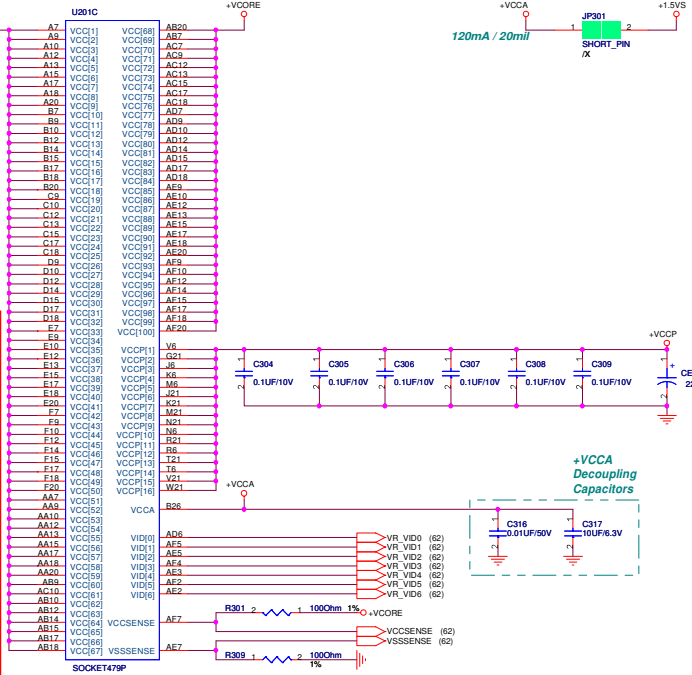
BCLK	FSB	BSEL#	BSEL1#	BSEL0
133	533	L	L	H
799	897	L	H	H

ASUS Title : Yonah CPU(1)
 Engineer: Spring Li
 Project Name: Custom 794Rp
 Date: #BBL/14.03.2008 Sheet 2 of 48

« Kennedy Zhang »



- +VCORE Low-Freq Capacitor**
Intel: 330UF *6
ATI: 330UF *6
R1F: 330UF *4
A7J: 330UF *5
- +VCORE Mid-Frequency Capacitor**
Intel: 22UF *32
ATI: 10UF *26
R1F: 22UF *16
A7J: 22UF*29 use 19
A6RF: 22UF*21 use 21
- +VCCP Decoupling Capacitor**
Intel: 270UF *1, 0.1UF *6
R1F: 270UF *1, 0.1UF *4
A7J: 220UF *1, 0.1UF *4
A6RF: 220UF *1, 0.1UF *6

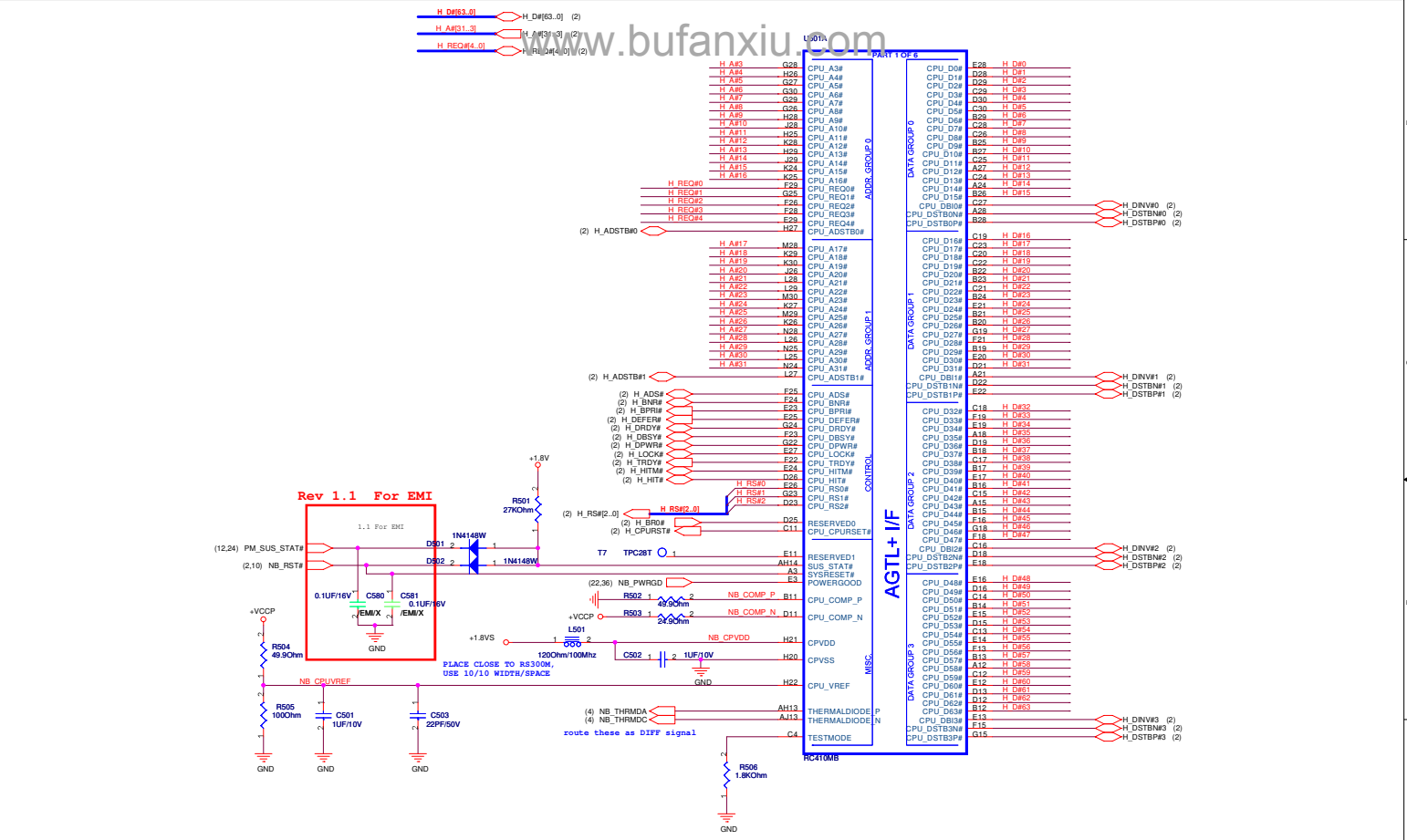


Layout note : route VCCSENSE and VSSSENSE trace at 27.4 Ohm with 2mil spacing mismatch and 18 mils trace on 7 mils spacing , please place the pull-up/down resistors within 1 inch of cpu

U201D		
A4	VSS11	P6
A5	VSS12	P21
A6	VSS13	P24
A7	VSS14	R2
A8	VSS15	R22
A9	VSS16	R22
A10	VSS17	R22
A11	VSS18	R22
A12	VSS19	R22
A13	VSS20	R22
A14	VSS21	R22
A15	VSS22	R22
A16	VSS23	R22
A17	VSS24	R22
A18	VSS25	R22
A19	VSS26	R22
A20	VSS27	R22
A21	VSS28	R22
A22	VSS29	R22
A23	VSS30	R22
A24	VSS31	R22
A25	VSS32	R22
A26	VSS33	R22
A27	VSS34	R22
A28	VSS35	R22
A29	VSS36	R22
A30	VSS37	R22
A31	VSS38	R22
A32	VSS39	R22
A33	VSS40	R22
A34	VSS41	R22
A35	VSS42	R22
A36	VSS43	R22
A37	VSS44	R22
A38	VSS45	R22
A39	VSS46	R22
A40	VSS47	R22
A41	VSS48	R22
A42	VSS49	R22
A43	VSS50	R22
A44	VSS51	R22
A45	VSS52	R22
A46	VSS53	R22
A47	VSS54	R22
A48	VSS55	R22
A49	VSS56	R22
A50	VSS57	R22
A51	VSS58	R22
A52	VSS59	R22
A53	VSS60	R22
A54	VSS61	R22
A55	VSS62	R22
A56	VSS63	R22
A57	VSS64	R22
A58	VSS65	R22
A59	VSS66	R22
A60	VSS67	R22
A61	VSS68	R22
A62	VSS69	R22
A63	VSS70	R22
A64	VSS71	R22
A65	VSS72	R22
A66	VSS73	R22
A67	VSS74	R22
A68	VSS75	R22
A69	VSS76	R22
A70	VSS77	R22
A71	VSS78	R22
A72	VSS79	R22
A73	VSS80	R22
A74	VSS81	R22
A75	VSS82	R22
A76	VSS83	R22
A77	VSS84	R22
A78	VSS85	R22
A79	VSS86	R22
A80	VSS87	R22
A81	VSS88	R22
A82	VSS89	R22
A83	VSS90	R22
A84	VSS91	R22
A85	VSS92	R22
A86	VSS93	R22
A87	VSS94	R22
A88	VSS95	R22
A89	VSS96	R22
A90	VSS97	R22
A91	VSS98	R22
A92	VSS99	R22
A93	VSS100	R22
A94	VSS101	R22
A95	VSS102	R22
A96	VSS103	R22
A97	VSS104	R22
A98	VSS105	R22
A99	VSS106	R22
A100	VSS107	R22
B1	VSS108	R22
B2	VSS109	R22
B3	VSS110	R22
B4	VSS111	R22
B5	VSS112	R22
B6	VSS113	R22
B7	VSS114	R22
B8	VSS115	R22
B9	VSS116	R22
B10	VSS117	R22
B11	VSS118	R22
B12	VSS119	R22
B13	VSS120	R22
B14	VSS121	R22
B15	VSS122	R22
B16	VSS123	R22
B17	VSS124	R22
B18	VSS125	R22
B19	VSS126	R22
B20	VSS127	R22
B21	VSS128	R22
B22	VSS129	R22
B23	VSS130	R22
B24	VSS131	R22
B25	VSS132	R22
B26	VSS133	R22
B27	VSS134	R22
B28	VSS135	R22
B29	VSS136	R22
B30	VSS137	R22
B31	VSS138	R22
B32	VSS139	R22
B33	VSS140	R22
B34	VSS141	R22
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B46	VSS153	R22
B47	VSS154	R22
B48	VSS155	R22
B49	VSS156	R22
B50	VSS157	R22
B51	VSS158	R22
B52	VSS159	R22
B53	VSS160	R22
B54	VSS161	R22
B55	VSS162	R22

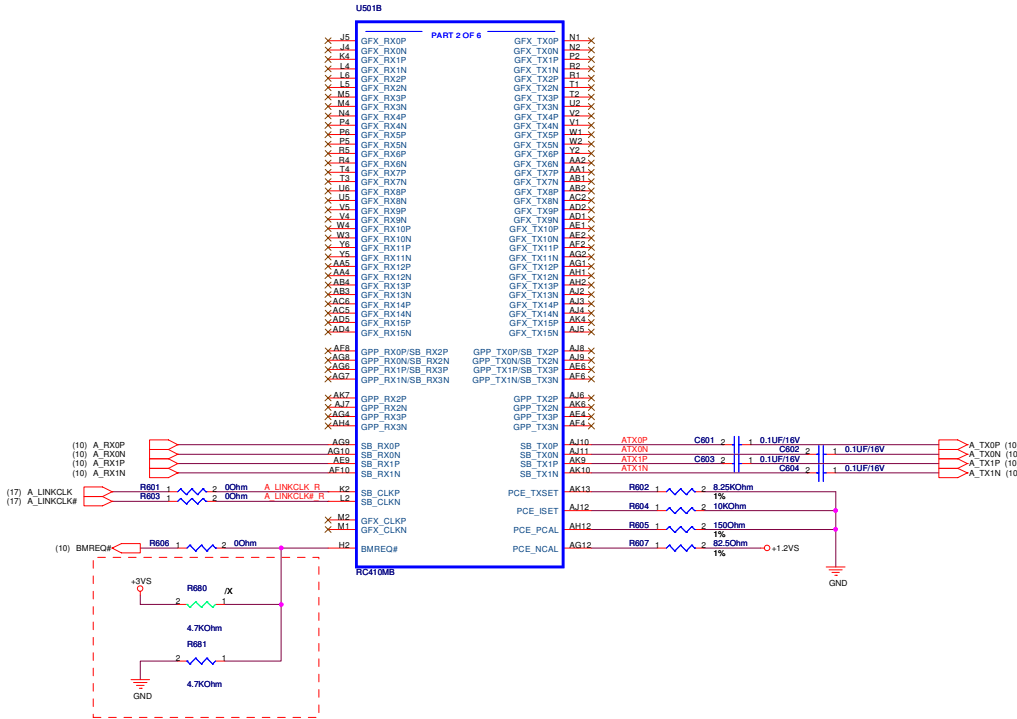
ASUS Title : Yonah CPU(2)
 <OrigName> Engineer: Spring LI
 Size Project Name
 Custom Z94Rp
 Date: 2008.11.03 2008 Sheet: 3 of 45

<< Kennedy_Zhang >>



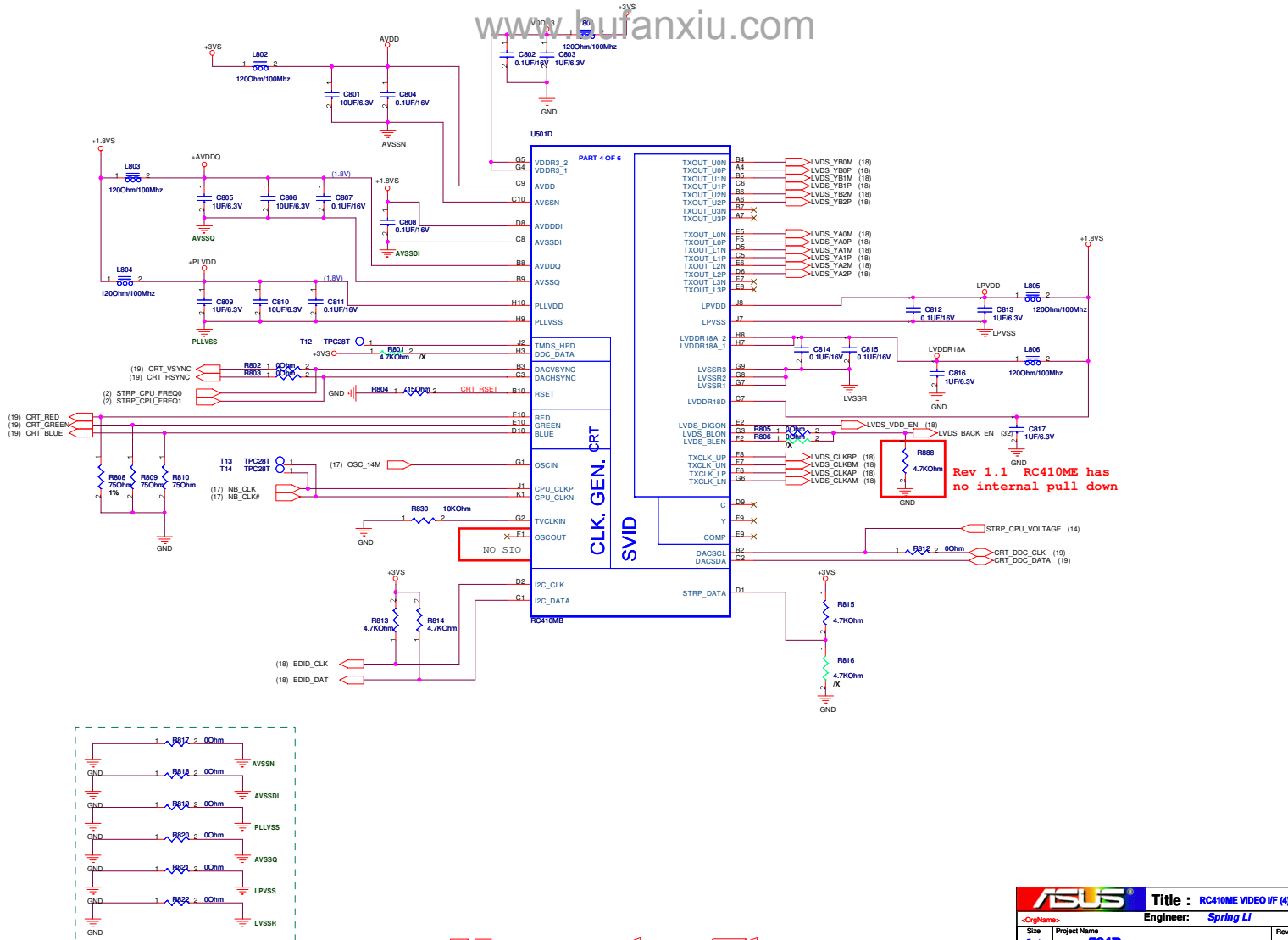
ASUS Title : RC410ME AGTL+ I/F(1)
 Engineer: Spring LI
 Project Name: Custom Z94Rp
 Date: 2014.03.03 2014 Sheet 5 of 45

<< Kennedy_Zhang >>

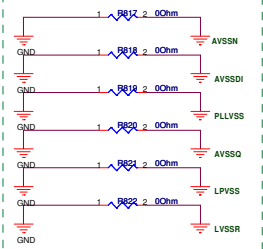


« Kennedy_Zhang »

ASUS		Title : RC410ME PCIE & A-Link2	
<OrigName>		Engineer: Spring LI	
Site	Project Name		Rev
Custom	Z94Rp		1.1
Date: 2024.11.03.2024		Sheet: 6	of 45

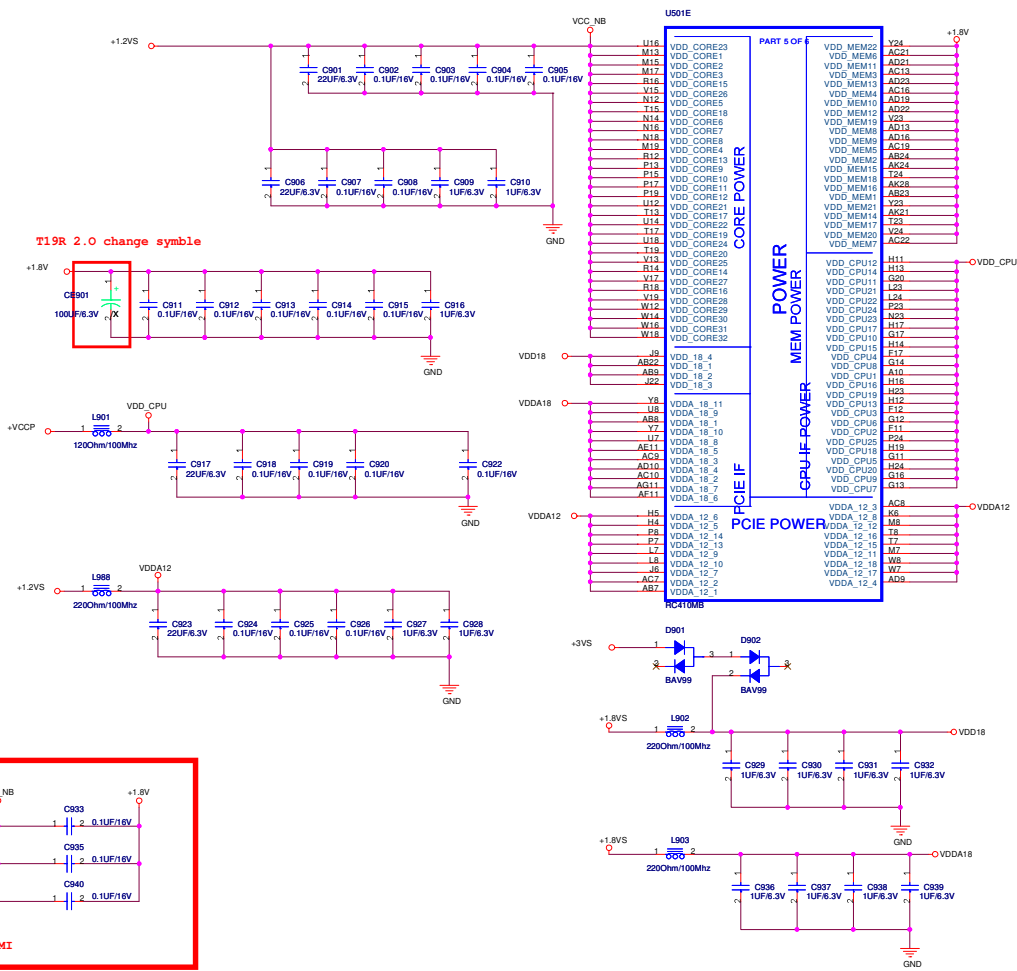


Rev 1.1 RC410ME has no internal pull down

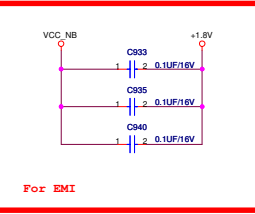


ASUS		Title : RC410ME VIDEO I/F (4)	
<OrigName>	Engineer: Spring Li	Size	Project Name
Custom	294Rp	Date: 2008.11.03.2008	Rev: 1.1
		Sheet: 8	of 45

<< Kennedy_Zhang >>



T19R 2.0 change symble

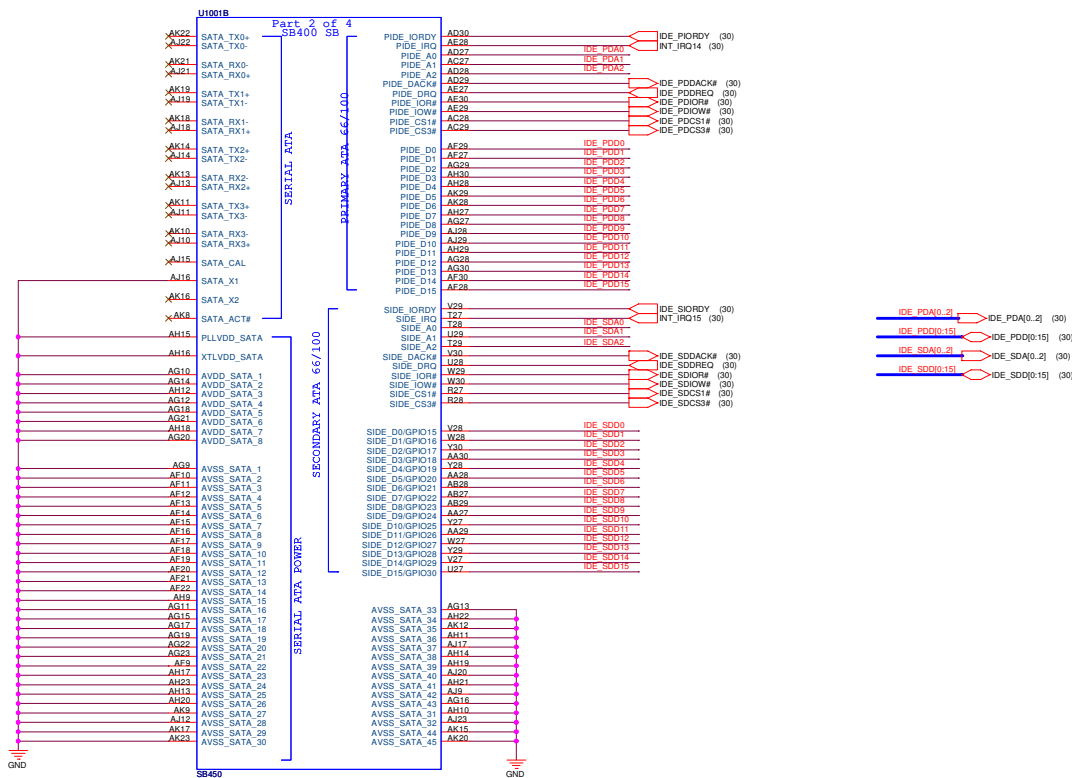


US01F

W5	VSSA40	PART 6 OF 6	VSS70	M14
M6	VSSA41		VSS71	AC14
AB5	VSSA44		VSS72	AG16
AB6	VSSA45		VSS73	AA2
VSS4	VSSA49		VSS74	A2
V7	VSSA38		VSS75	D27
AA1	AC06		VSS76	AC06
AA7	VSSA3		VSS77	H18
AA8	VSSA2		VSS78	A16
AD7	VSSA6		VSS79	AD17
AD8	VSSA5		VSS80	R2
BB	VSSA33		VSS81	B27
BB1	VSSA29		VSS82	D25
BB2	VSSA28		VSS83	R20
B7	VSSA22		VSS84	VSS9
AD9	VSSA13		VSS85	VSS10
AA6	VSSA10		VSS86	VSS11
AA5	VSSA9		VSS87	VSS12
AA4	VSSA8		VSS88	VSS13
AA3	VSSA7		VSS89	VSS14
AA2	VSSA6		VSS90	VSS15
AA1	VSSA5		VSS91	VSS16
AA0	VSSA4		VSS92	VSS17
AA	VSSA3		VSS93	VSS18
AA	VSSA2		VSS94	VSS19
AA	VSSA1		VSS95	VSS20
AA	VSSA0		VSS96	VSS21
AA	VSSA0		VSS97	VSS22
AA	VSSA0		VSS98	VSS23
AA	VSSA0		VSS99	VSS24
AA	VSSA0		VSS100	VSS25
AA	VSSA0		VSS101	VSS26
AA	VSSA0		VSS102	VSS27
AA	VSSA0		VSS103	VSS28
AA	VSSA0		VSS104	VSS29
AA	VSSA0		VSS105	VSS30
AA	VSSA0		VSS106	VSS31
AA	VSSA0		VSS107	VSS32
AA	VSSA0		VSS108	VSS33
AA	VSSA0		VSS109	VSS34
AA	VSSA0		VSS110	VSS35
AA	VSSA0		VSS111	VSS36
AA	VSSA0		VSS112	VSS37
AA	VSSA0		VSS113	VSS38
AA	VSSA0		VSS114	VSS39
AA	VSSA0		VSS115	VSS40
AA	VSSA0		VSS116	VSS41
AA	VSSA0		VSS117	VSS42
AA	VSSA0		VSS118	VSS43
AA	VSSA0		VSS119	VSS44
AA	VSSA0		VSS120	VSS45
AA	VSSA0		VSS121	VSS46
AA	VSSA0		VSS122	VSS47
AA	VSSA0		VSS123	VSS48
AA	VSSA0		VSS124	VSS49
AA	VSSA0		VSS125	VSS50
AA	VSSA0		VSS126	VSS51
AA	VSSA0		VSS127	VSS52
AA	VSSA0		VSS128	VSS53
AA	VSSA0		VSS129	VSS54
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AA	VSSA0		VSS131	VSS56
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AA	VSSA0		VSS133	VSS58
AA	VSSA0		VSS134	VSS59
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AA	VSSA0		VSS136	VSS61
AA	VSSA0		VSS137	VSS62
AA	VSSA0		VSS138	VSS63
AA	VSSA0		VSS139	VSS64
AA	VSSA0		VSS140	VSS65
AA	VSSA0		VSS141	VSS66
AA	VSSA0		VSS142	VSS67
AA	VSSA0		VSS143	VSS68
AA	VSSA0		VSS144	VSS69
AA	VSSA0		VSS145	VSS70
AA	VSSA0		VSS146	VSS71
AA	VSSA0		VSS147	VSS72
AA	VSSA0		VSS148	VSS73
AA	VSSA0		VSS149	VSS74
AA	VSSA0		VSS150	VSS75
AA	VSSA0		VSS151	VSS76
AA	VSSA0		VSS152	VSS77
AA	VSSA0		VSS153	VSS78
AA	VSSA0		VSS154	VSS79
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AA	VSSA0		VSS167	VSS92
AA	VSSA0		VSS168	VSS93
AA	VSSA0		VSS169	VSS94
AA	VSSA0		VSS170	VSS95
AA	VSSA0		VSS171	VSS96
AA	VSSA0		VSS172	VSS97
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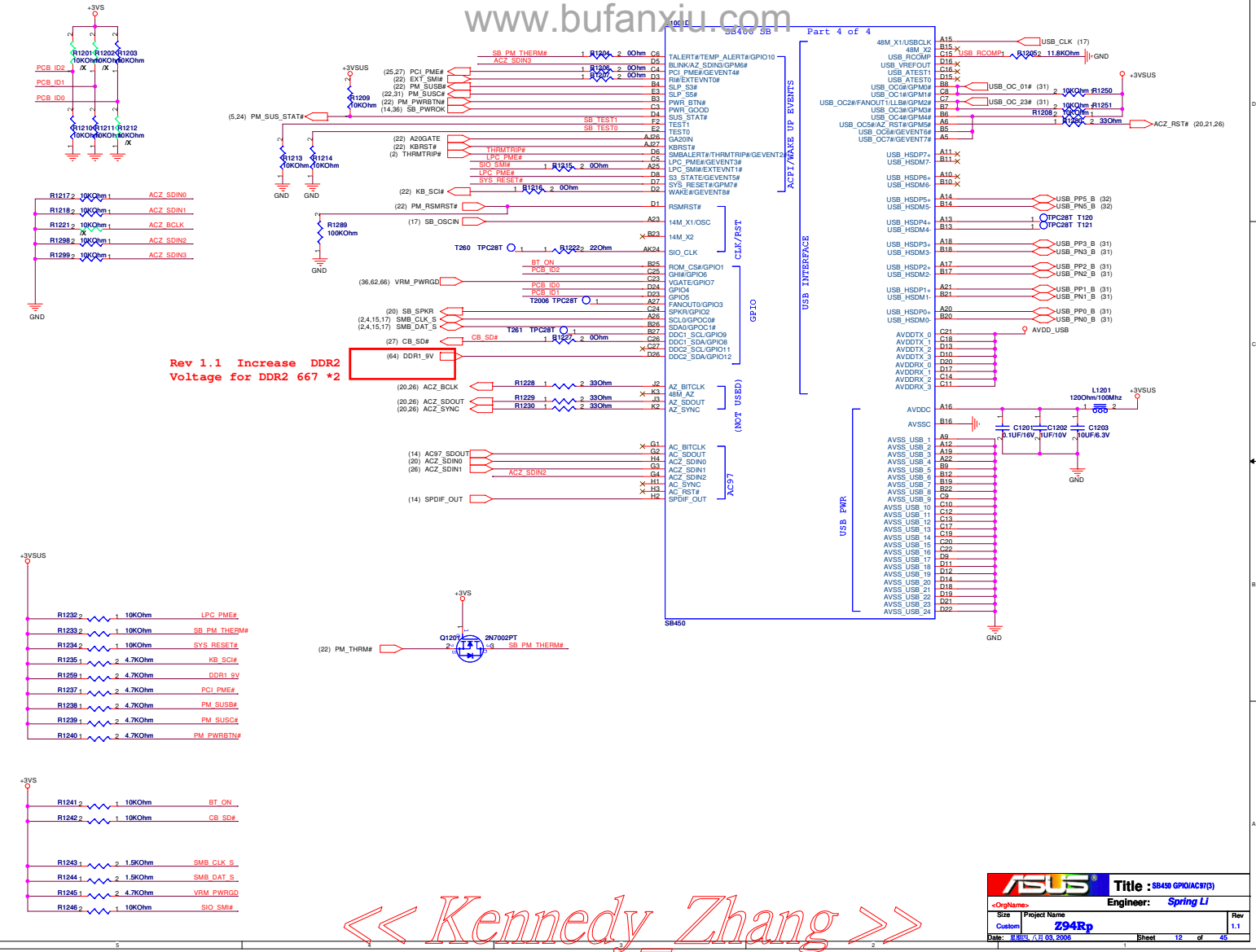
ASUS Title : RC410ME POWER (5)
 Engineer : Spring Li
 Project Name : Z94Rp
 Date : 1-25-2016 Sheet : 9 of 46

« Kennedy_Zhang »



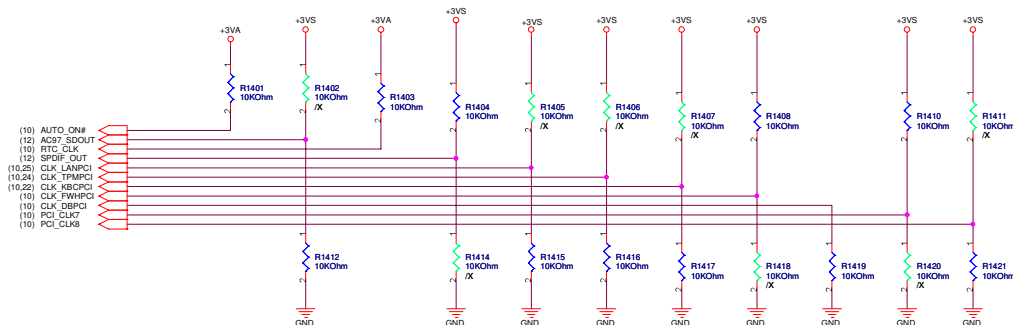
« Kennedy_Zhang »

ASUS		Title : SB450 IDE (2)
<OrigName>		Engineer: Spring LI
Size	Project Name	Rev
Custom	Z94Rp	1.1
Date: 4/24/06	Sheet	11 of 45



<< Kennedy_Zhang >>

ASUS		Title : SB450 GPIOAC97(B)	
<OrigName>	Project Name	Engineer:	Spring Li
State	294Rp	Date:	8/28/2005
Sheet	12	of	45



REQUIRED STRAPS

	AUTO_ON#	AC_SDOOUT	RTC_CLK	SPDF_OUT	CLK_LAN	CLK_SIO	CLK_KB	CLK_FW	CLK_DB	PCI_CLK7	PCI_CLK8
PULL HIGH	MANUAL PWR ON	USE DEBUG STRAPS	INTERNAL RTC	SIO 24MHz		SEE NOTE1	USE USB PLL		CPU I/F = K8	ROM TYPE H.H = PCI ROM	
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	SIO 48MHz		USB PHY PWRDOWN ENABLE	BYPASS USB PLL	SEE NOTE2	CPU I/F = P4	H.L = LPC ROM I DEFAULT LPC Address Mapped below 1M L.H = LPC ROM II LPC Address Mapped to top 4G L.L = FW ROM	

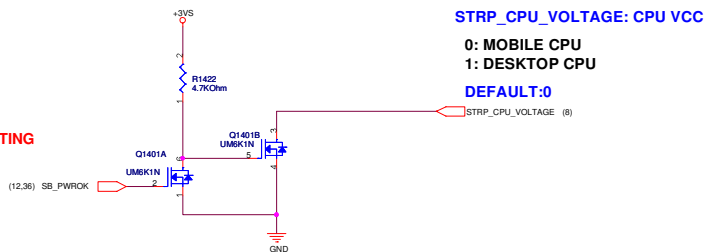
NOTE

1. USB CLK STRAPPING CHANGE

	A21,A22,A23	A31 AND NEWER
10K PULL UP	OSC/CLOCK BUFFER	CRYSTAL PAD
10K PULL DOWN	CRYSTAL PAD	OSC/CLOCK BUFFER

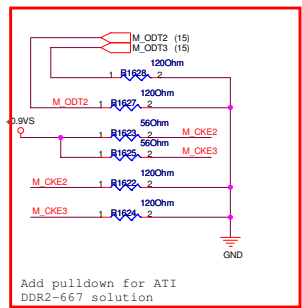
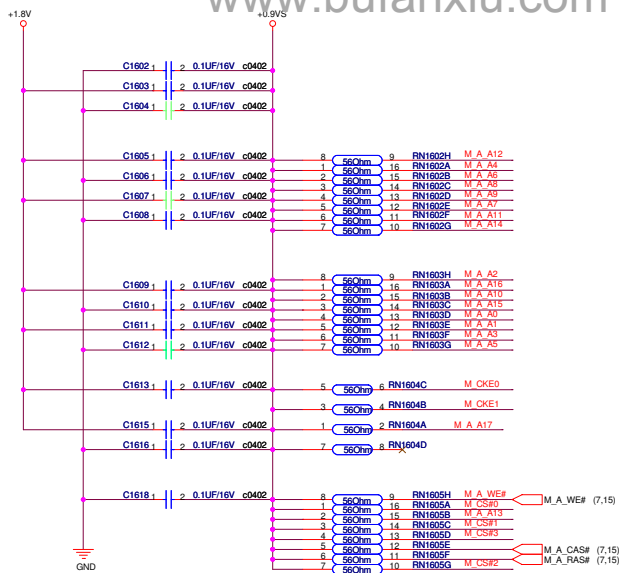
2. 14MHz CLOCK TYPE STRAPPING

	A11~A31	A32 AND ABOVE
	14MHz CLOCK PAD IS CRYSTAL PAD	PCIE COMMON MODE SETTING
10K PULL UP	CLOCK INPUT BUFFER	PCIE CM_SET LOW
10K PULL DOWN	CRYSTAL PAD	PCIE CM_SET HIGH

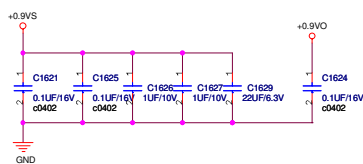


ASUS Title : SB450 STRAPS(5)
 Engineer: Spring LJ
 Project Name: Z94Rp
 Date: 2008.6.18.09.2008 Sheet 14 of 45

« Kennedy_Zhang »



Add pulldown for ATI DDR2-667 solution

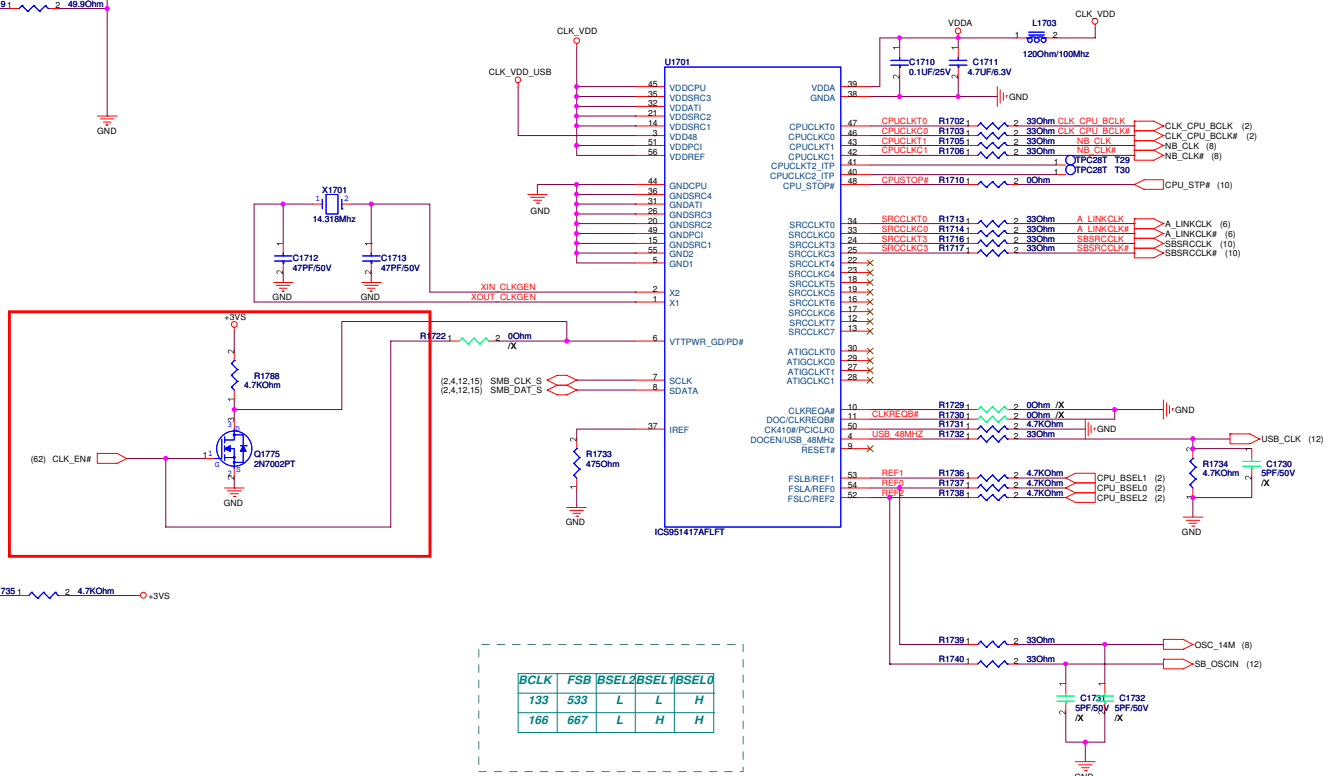


ASUS		Title : DDR2 Termination
Engineer: Spring LI		
<OrigName>	Project Name	Rev
Custom	Z94Rp	1.1
Date: 2008/03/03	Sheet 16	of 45

<< Kennedy_Zhang >>

PLACE termination close to source IC

- CLK_CPU_BCLK R1701 2 49.90Ohm
- CLK_CPU_BCLK# R1704 2 49.90Ohm
- NB_CLK R1708 2 49.90Ohm
- NB_CLK# R1711 2 49.90Ohm
- A_LINKCLK R1712 2 49.90Ohm
- A_LINKCLK# R1715 2 49.90Ohm
- SBSRCCLK R1718 2 49.90Ohm
- SBSRCCLK# R1719 2 49.90Ohm

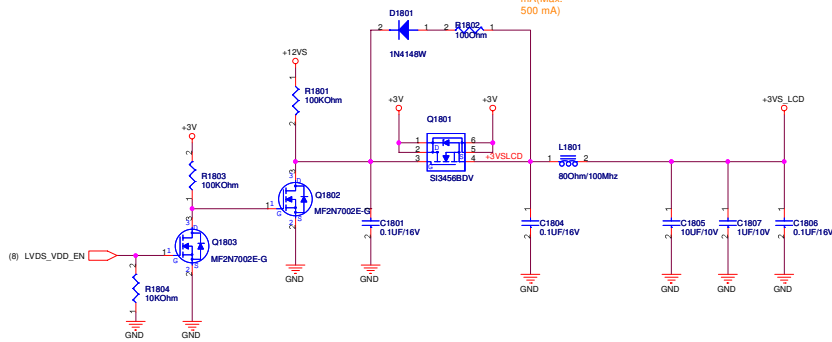


BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

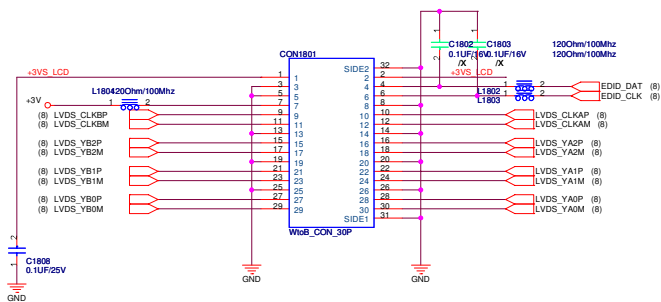
ASUS		Title : CLOCK GENERATOR	
-<OrigName>		Engineer: Spring Li	
Size	Project Name		Rev
Custom	Z94Rp		1.1
Date:	星期日 八月 03 2008	Sheet	17 of 45

« Kennedy_Zhang »

LCD Power



Full
Active:
410
mA(Max.
500 mA)

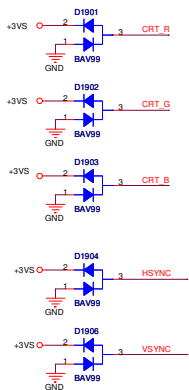


Cable Requirement:
Impedance: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

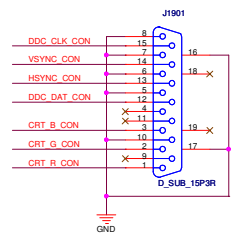
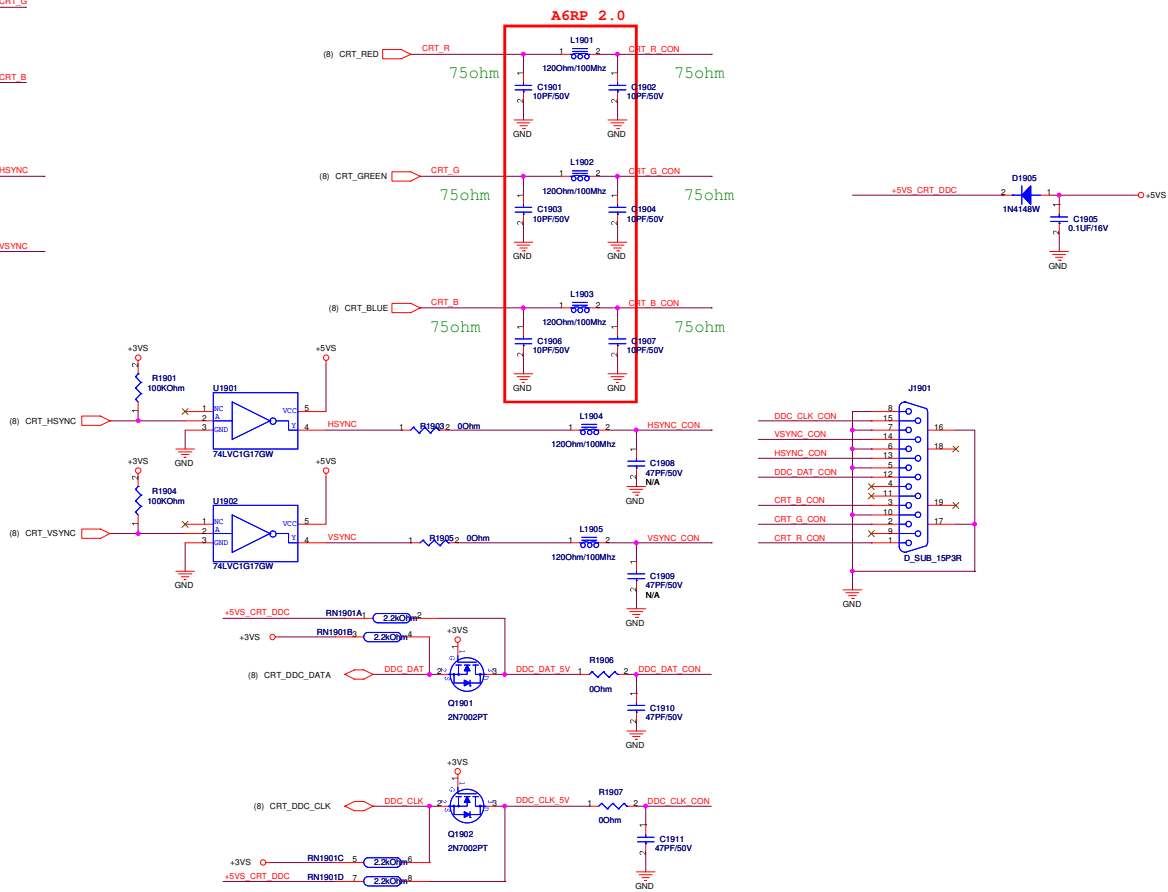
LCD LVDS Interface

ASUS		Title : LVDS & INVERTER (CAMERA)	
<OrigName>		Engineer: Spring Li	
Site	Project Name		Rev
Custom	Z94Rp		1.1
Date: 2008.11.03.2008		Sheet: 18	of 48

<< Kennedy_Zhang >>

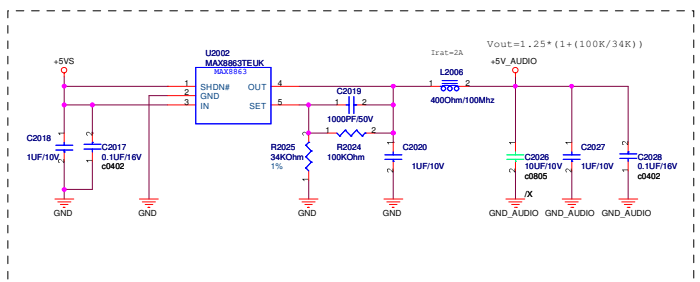
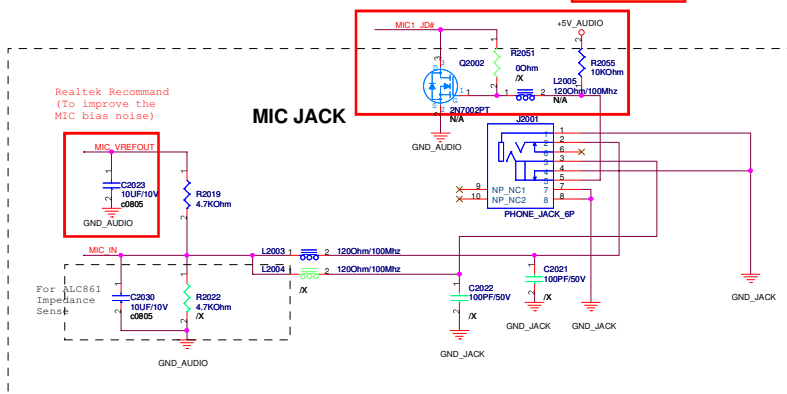
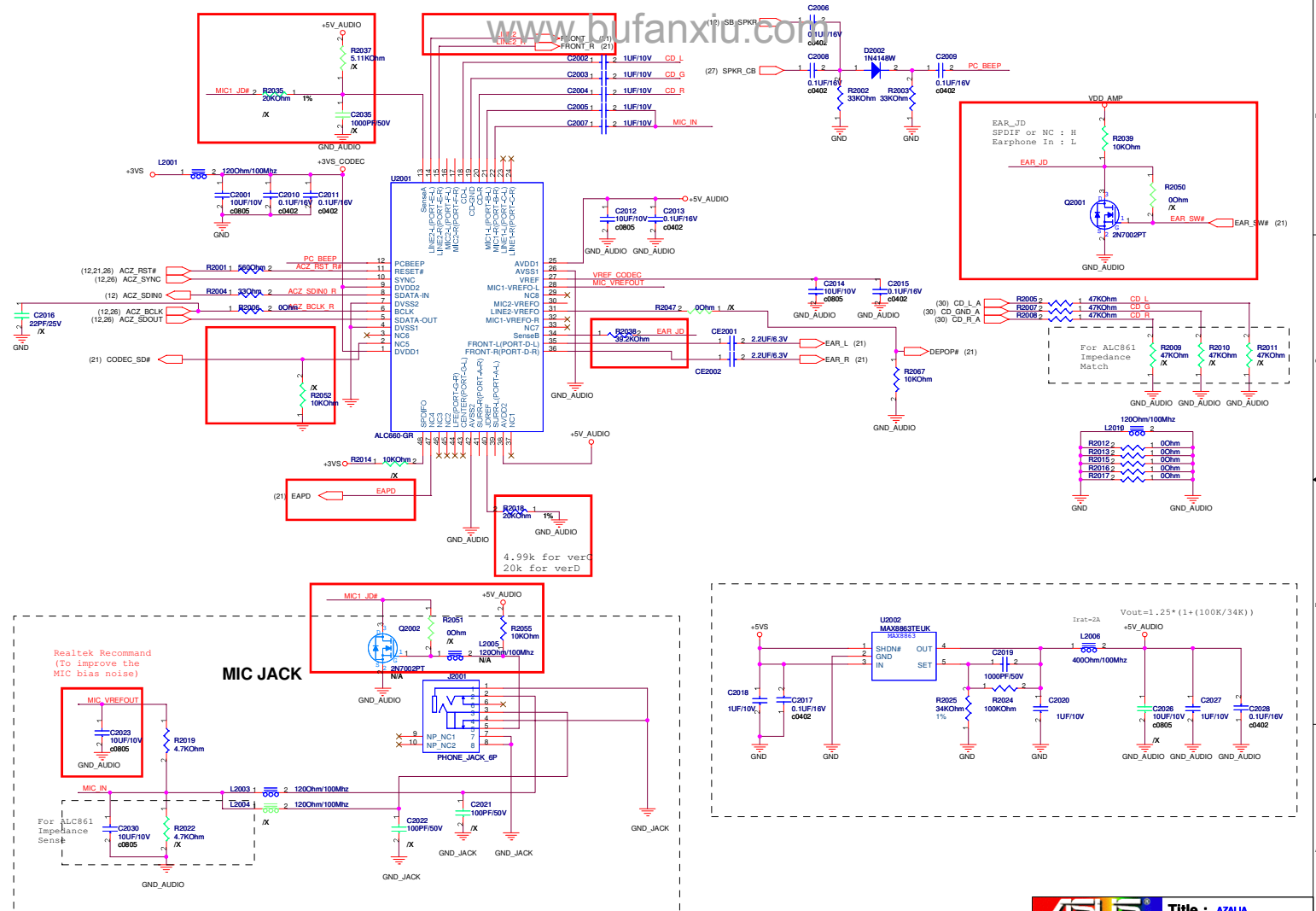


PLACE ESD Diodes near VGA port



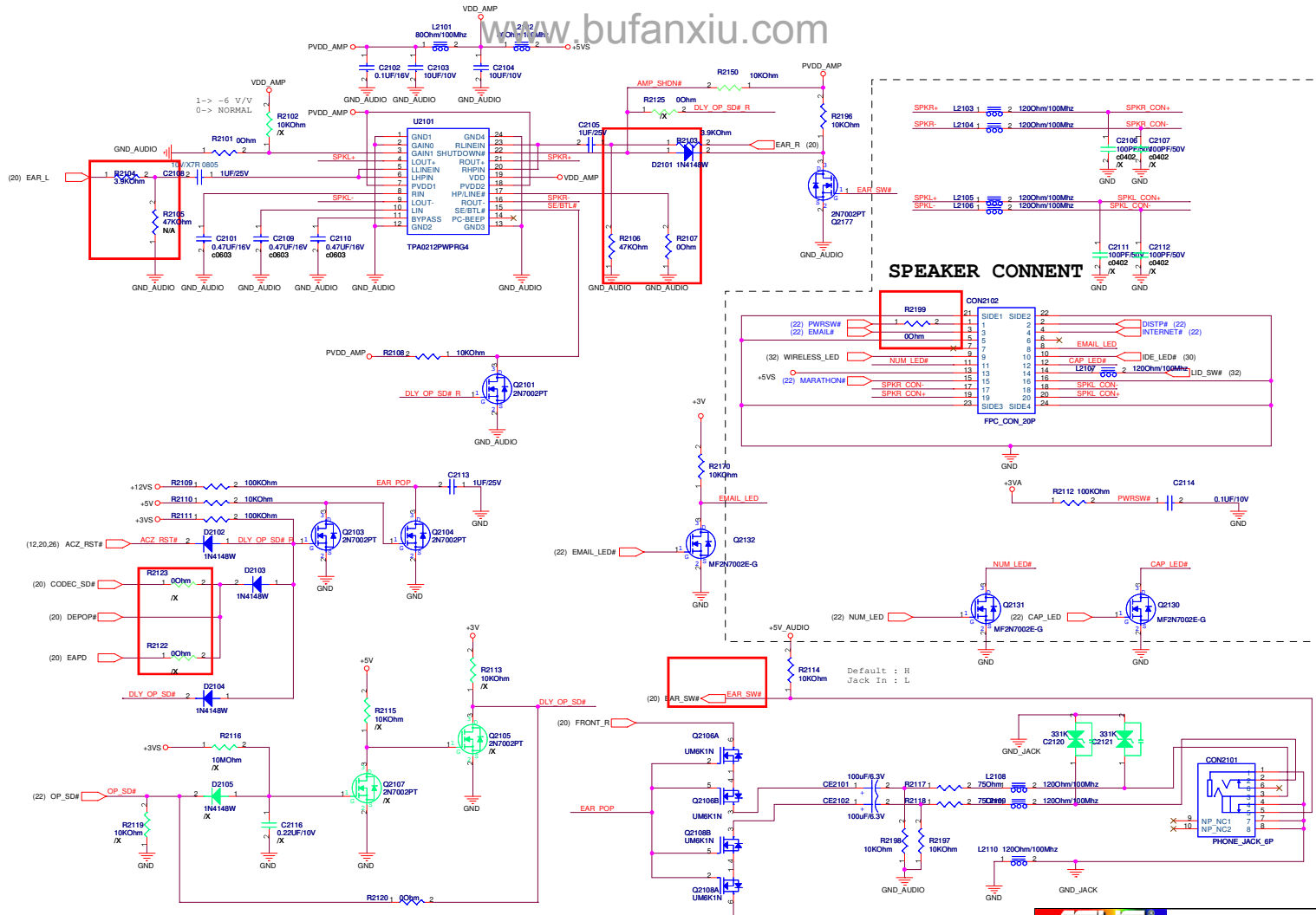
« Kennedy_Zhang »

ASUS		Title : CRT CONNECTOR	
<OrigName>		Engineer: Spring LI	
Site	Project Name		Rev
Custom	294Rp		1.1
Date: 8/26/2008 11:03:20AM		Sheet: 19	of 48

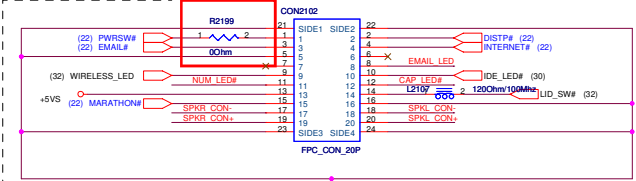


ASUS		Title : AZALIA
<OrigName>	Project Name	Engineer: Spring LI
Size	Custom	294Rp
Date: 8/11/2018	Sheet	20 of 48

<< Kennedy_Zhang >>

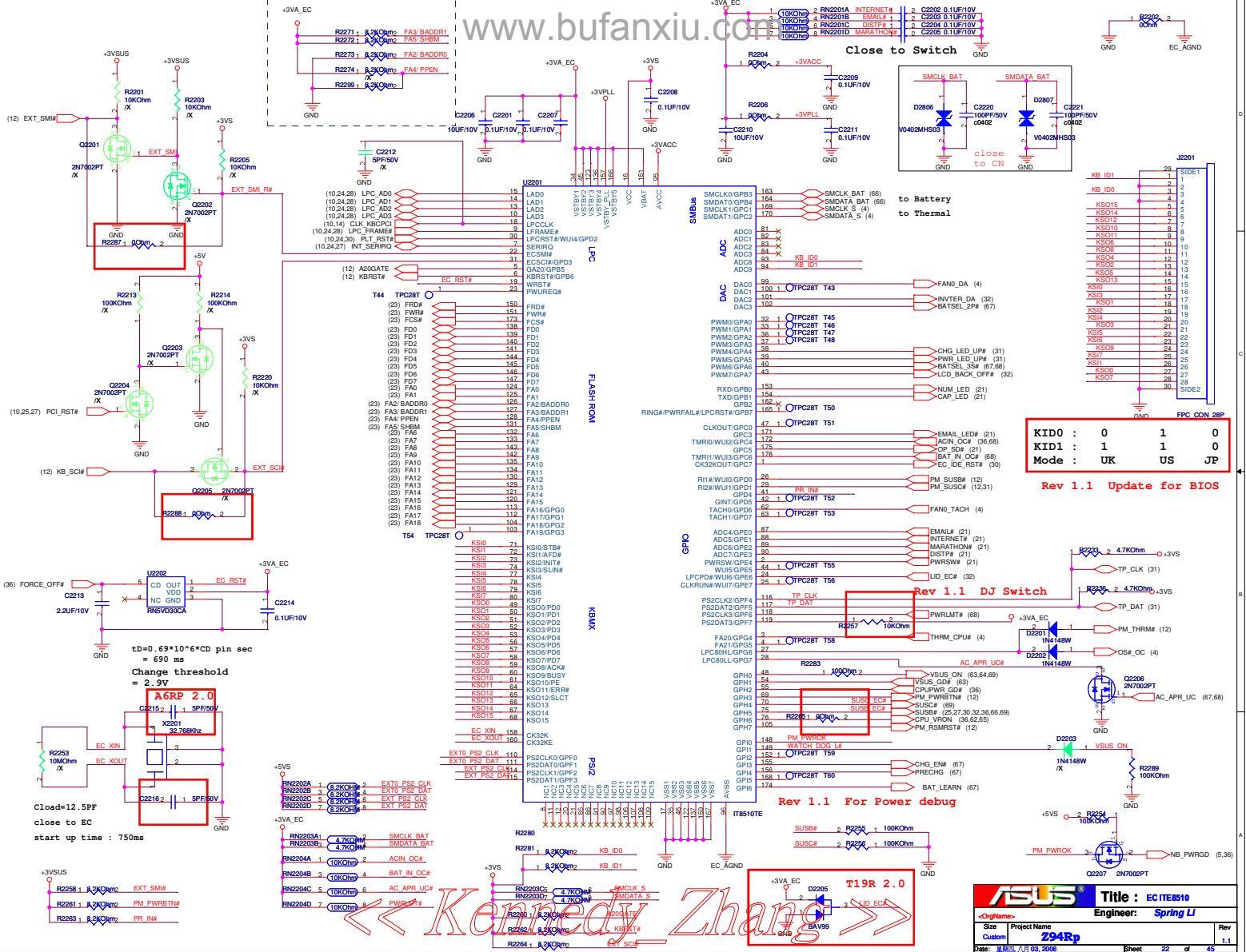


SPEAKER CONNENT



ASUS		Title : AMPLIFIER 2 CHANNEL	
<<OrigName>>	Project Name	Engineer:	Spring Li
Size	Custom	Customer	294Rp
Date: 8/11	3.1.12.2009	Sheet	21 of 46

<< Kennedy_Zhang >>



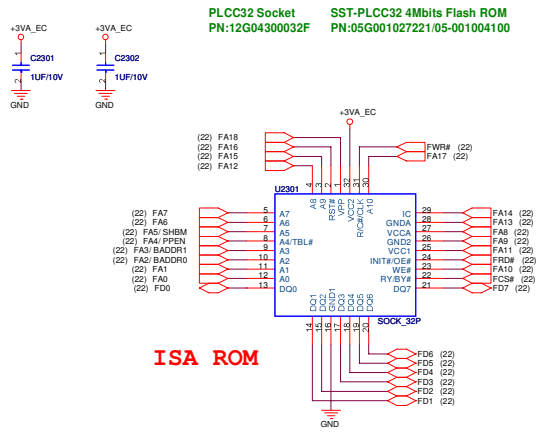
Rev 1.1 Update for BIOS

KID0 :	0	1	0
KID1 :	1	1	0
Mode :	UK	US	JP

Rev 1.1 DJ Switch

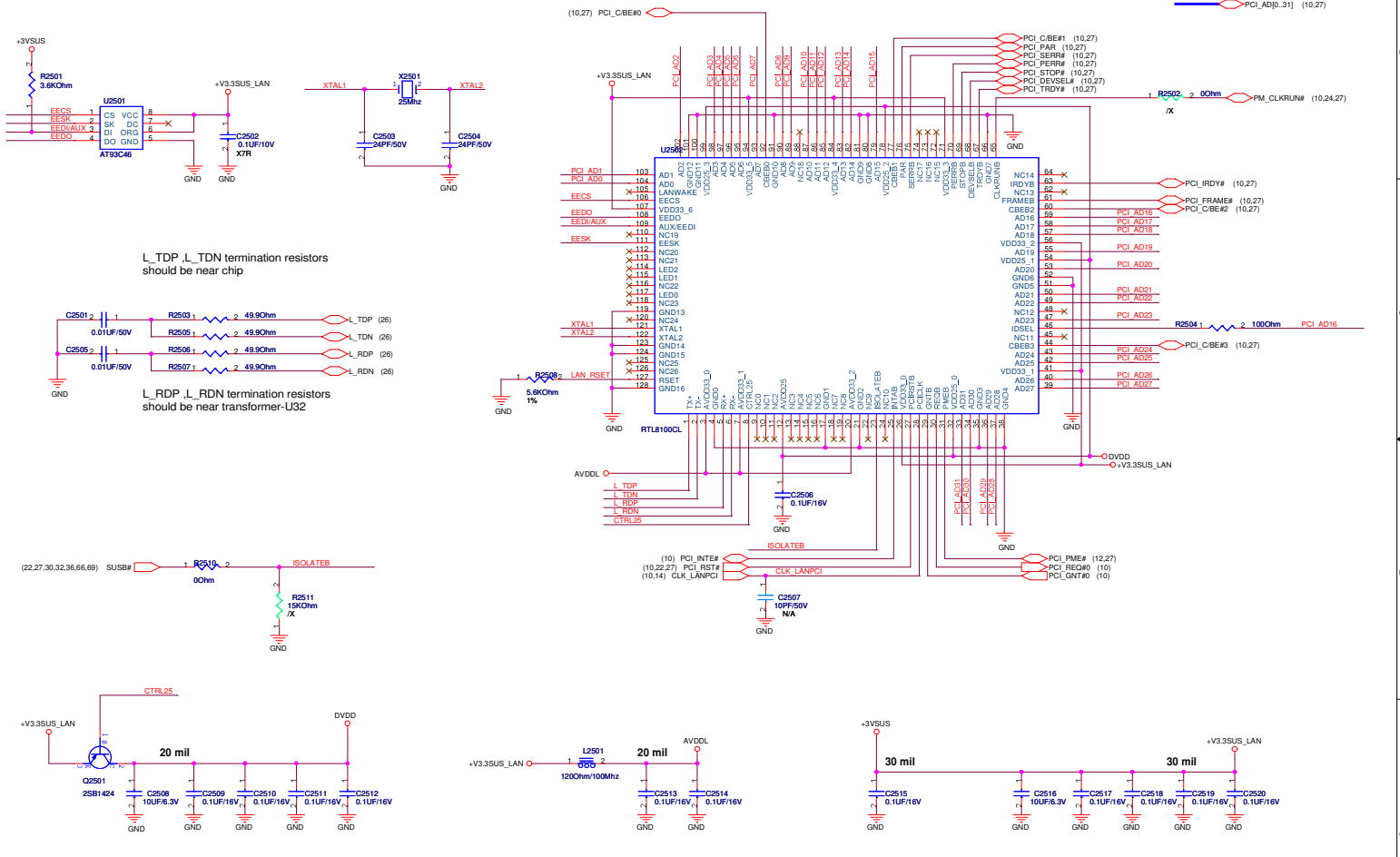
Rev 1.1 For Power debug

ASUS		Title :	EC1TE8510
Size	Project Name	Engineer :	Spring LI
Custom	Z94Rp		
Date :	#REV# 7/18/03_2006	Sheet	22 of 45
		Rev	1.1



ASUS		Title : ISA ROM & SPI ROM	
<OrigName>		Engineer: Spring LI	
Site	Project Name	Rev	
Custom	Z94Rp	1.1	
Date: 2008.11.03.2008		Sheet	23 of 45

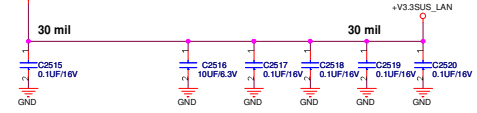
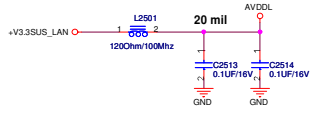
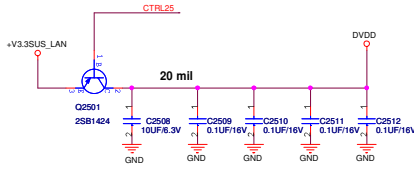
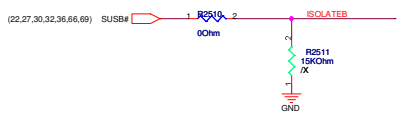
« Kennedy_Zhang »



L_TDP_L_TDN termination resistors should be near chip



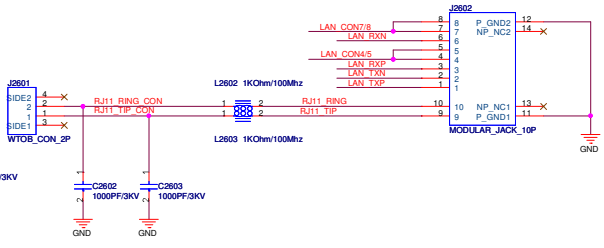
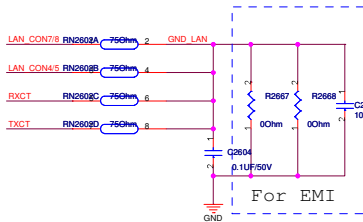
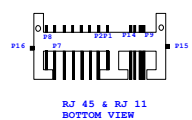
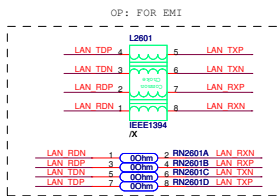
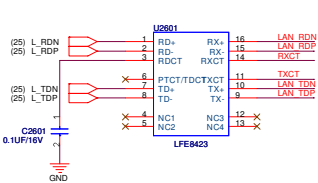
L_RDP_L_RDN termination resistors should be near transformer-U32



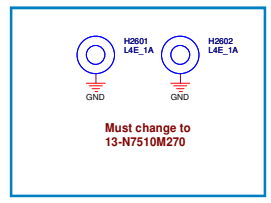
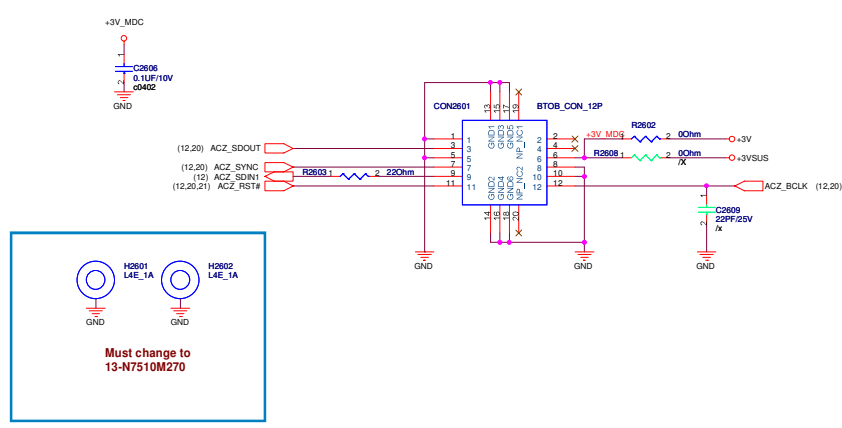
ASUS		Title : LAN_8100CL
OrigName:	Project Name	Engineer: Spring Li
Site:	Customer	Rev 1.1
Date: 8/18/2009	Sheet	25 of 46

« Kennedy_Zhang »

LAN PORT

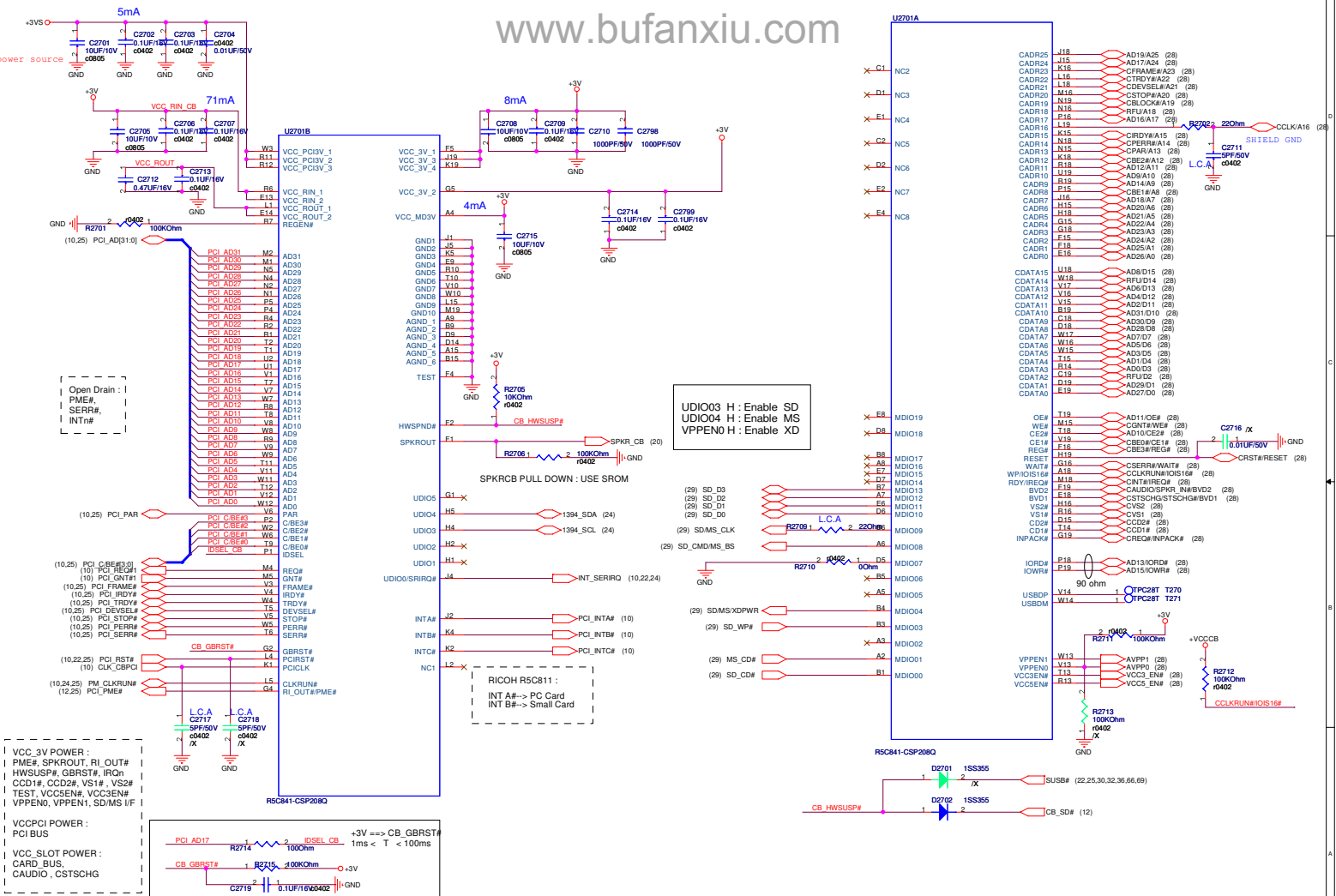


MDC



ASUS		Title : RJ11+45 & MDC	
<OrigName>	Project Name	Engineer:	Spring LI
Site	Custom	294Rp	Rev 1.1
Date:	2024.11.03.2024	Sheet	26 of 45

<< Kennedy_Zhang >>



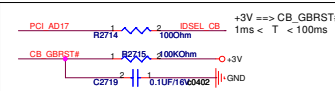
UDIO03 H : Enable SD
 UDIO04 H : Enable MS
 VPPEN0 H : Enable XD

RICOH R5C811 :
 INT A# -> PC Card
 INT B# -> Small Card

VCC_3V POWER :
 PME#, SPKR_OUT, RI_OUT#
 HWSUSP#, GBRST#, IRQn
 CCB1#, CCB2#, VS1#, VS2#
 TEST, VCCSEN#, VCCSEN#
 VPPEN0, VPPEN1, SD/MS I/F

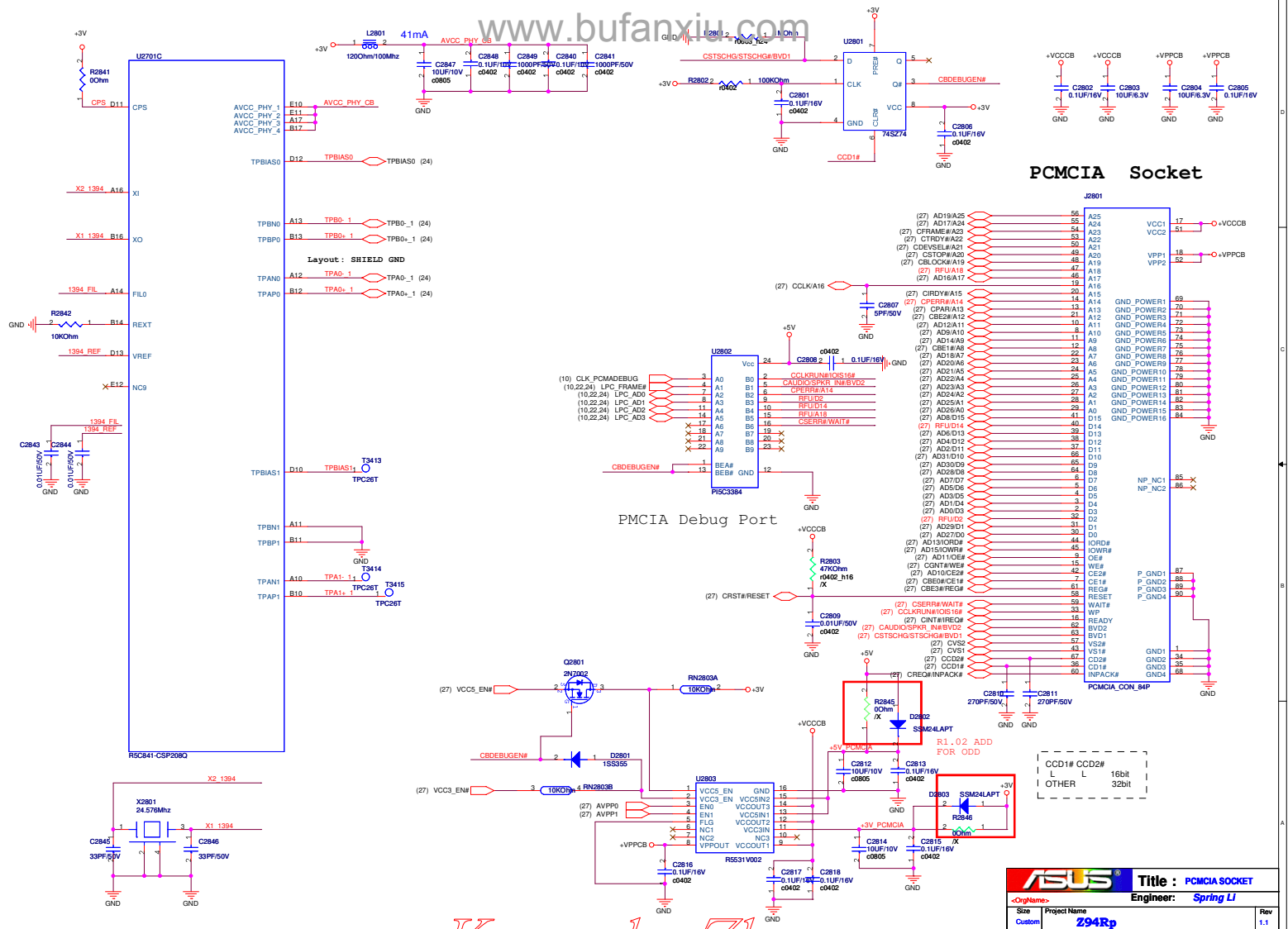
VCCPCI POWER :
 PCI BUS

VCC_SLOT POWER :
 CARD_BUS,
 CAUDIO, CSTSCHG



ASUS		Title : CARDBUS RICOH RSC841	
<OrigName>		Engineer: Spring Li	
Size	Project Name	Rev	
Custom	294Rp	1.1	
Date: 2008.11.03.2008		Sheet: 27	of 45

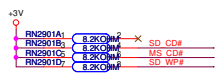
<< Kennedy_Zhang >>



« Kennedy_Zhang »

ASUS Title : PCMCIA SOCKET
 Engineer: Spring Li

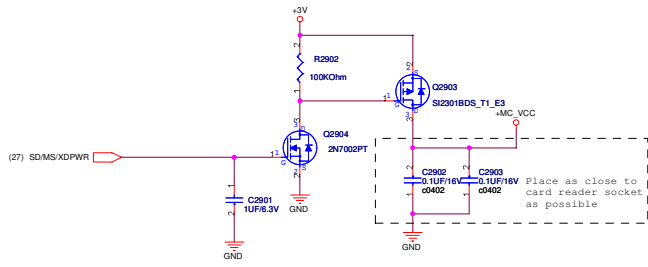
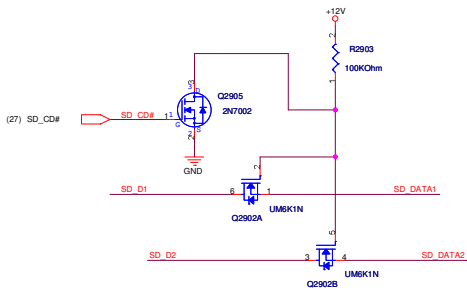
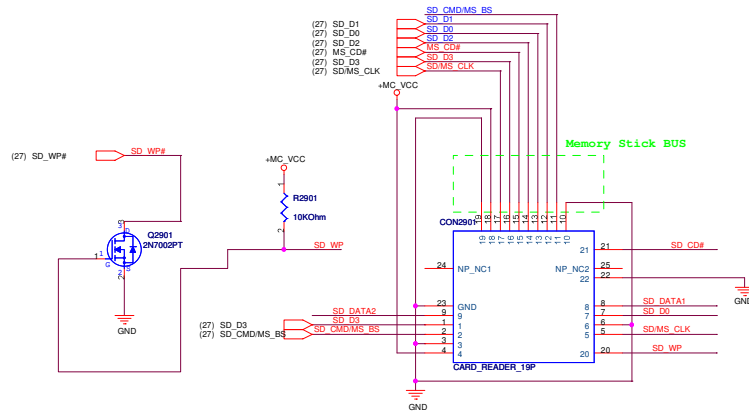
Size	Project Name	Rev
Custom	294Rp	1.1
Date: 2008.11.03.2008	Sheet	28 of 45



Memory Card Detect

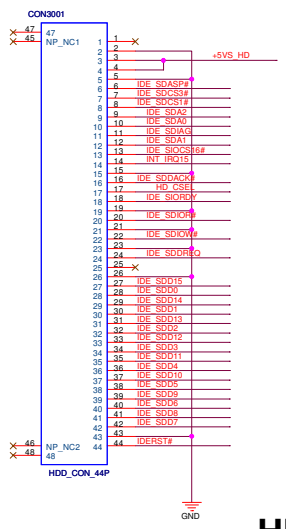
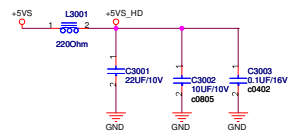
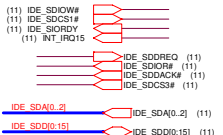
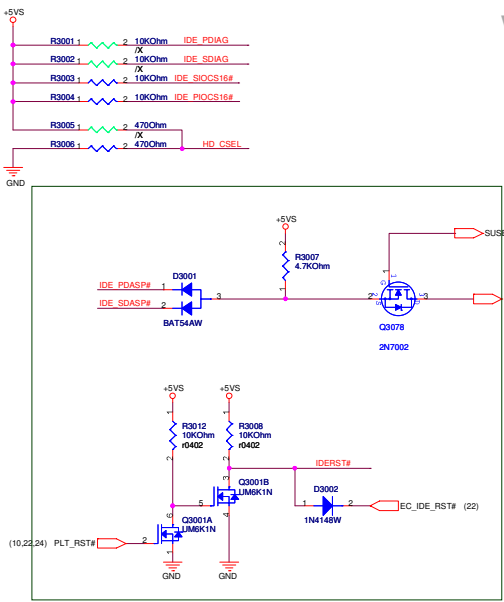
MS_CD#	SD_CD#	Not Support
0	0	Not Support
1	0	Small Card
1	1	Memory Stick

MC_CD# : Memory Card Detect

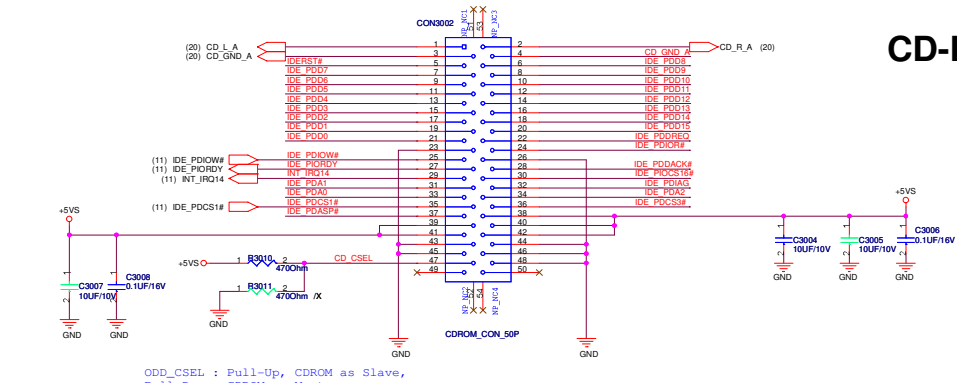


ASUS		Title : 4IN 1 CON
Project Name		Engineer: Spring LI
Site	Custom	Rev 1.1
Date: 11/23/2008		Sheet 29 of 45

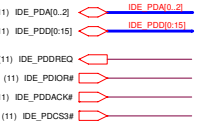
« Kennedy_Zhang »



HDD



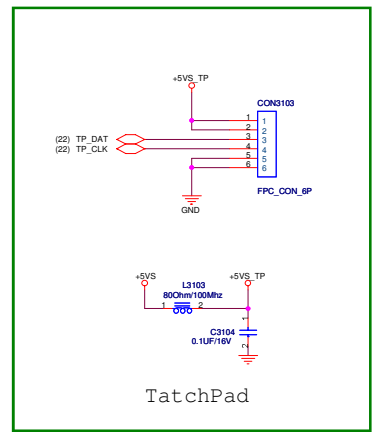
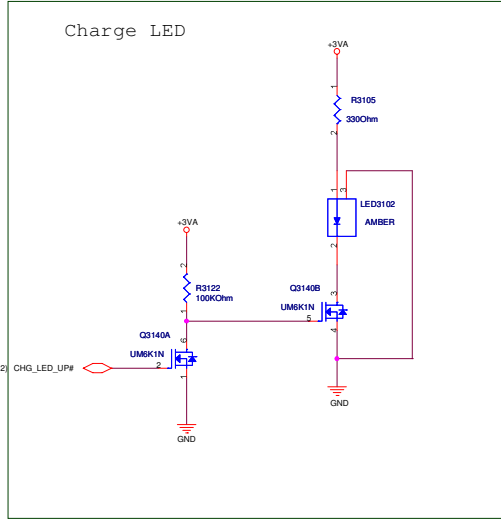
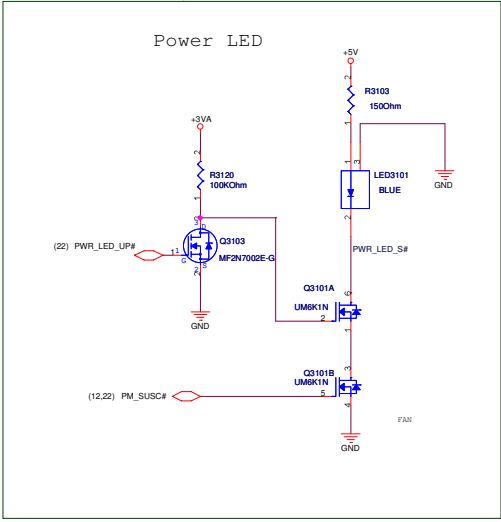
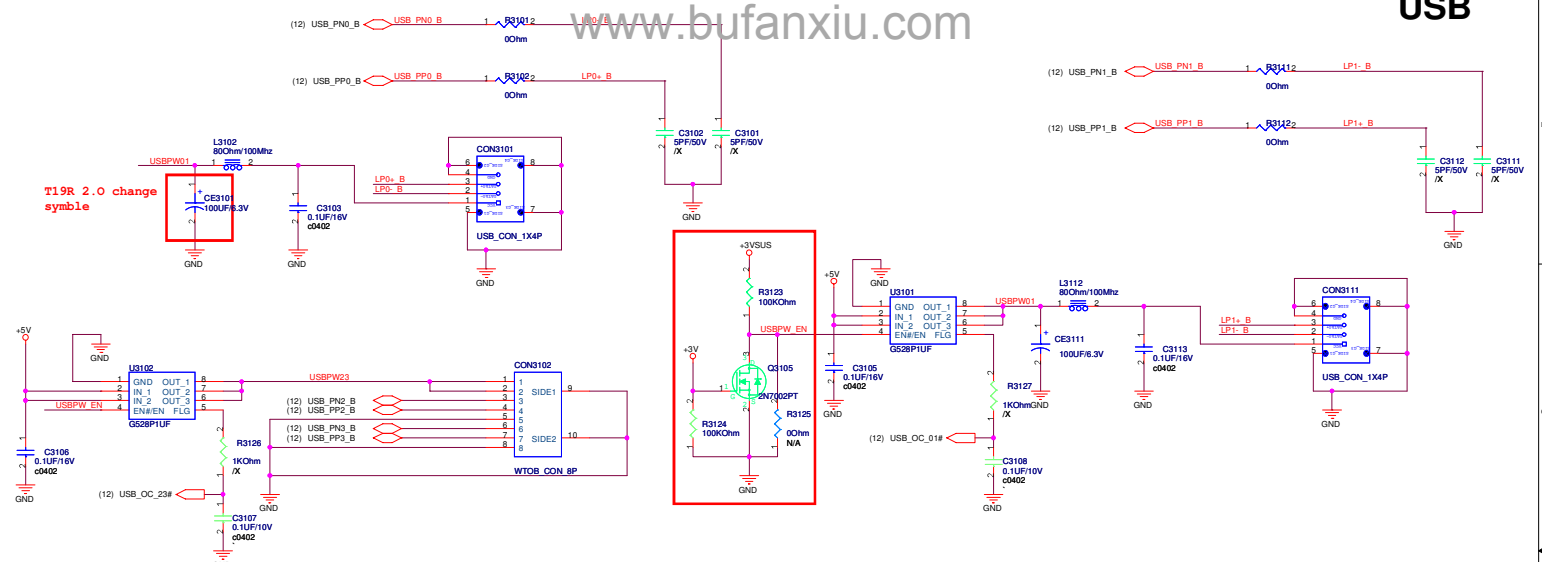
CD-ROM



ODD_CSEL : Pull-Up, CDROM as Slave, Pull-Down, CDROM as Master

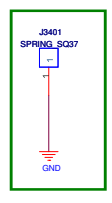
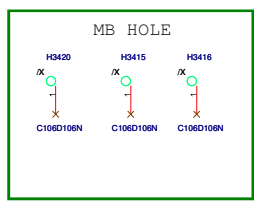
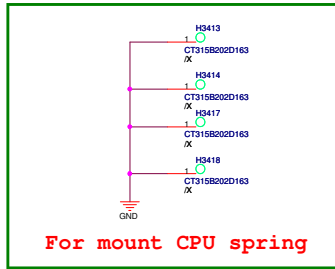
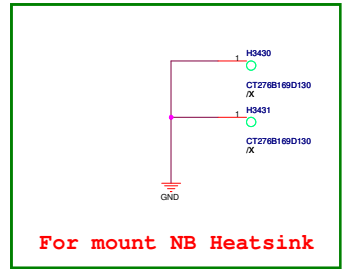
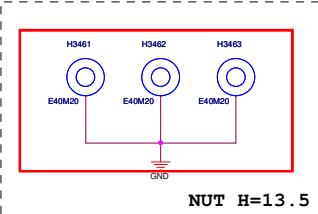
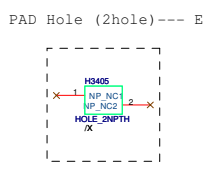
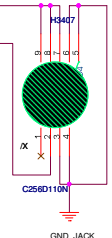
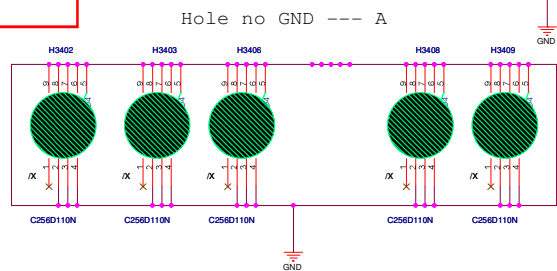
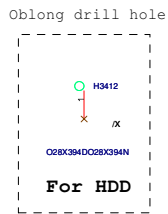
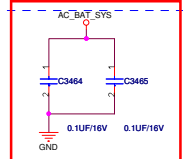
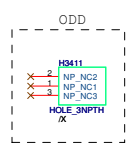
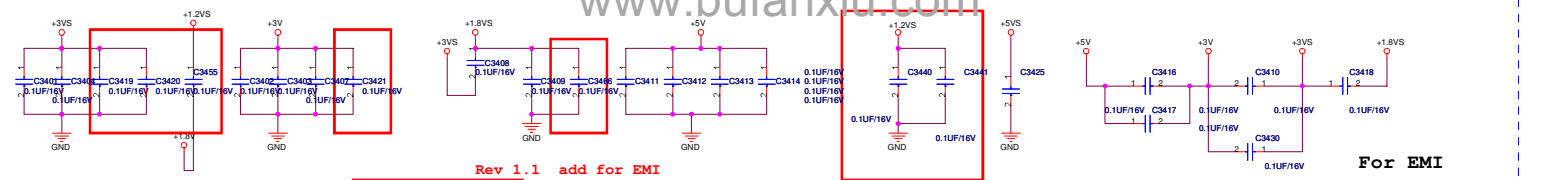
		Title : HDD & CD-ROM	
Engineer: Spring Li		Rev: 1.1	
Size: Custom	Project Name: 794Rp	Date: 2008.10.03	Sheet: 30 of 45

« Kennedy_Zhang »



ASUS		Title : USB / LED / TP	
<<OrigName>>		Engineer: Spring LI	
Site	Project Name	Rev	
Custom	Z94Rp	1.1	
Date: 8/18/2009	Sheet	31	of 46

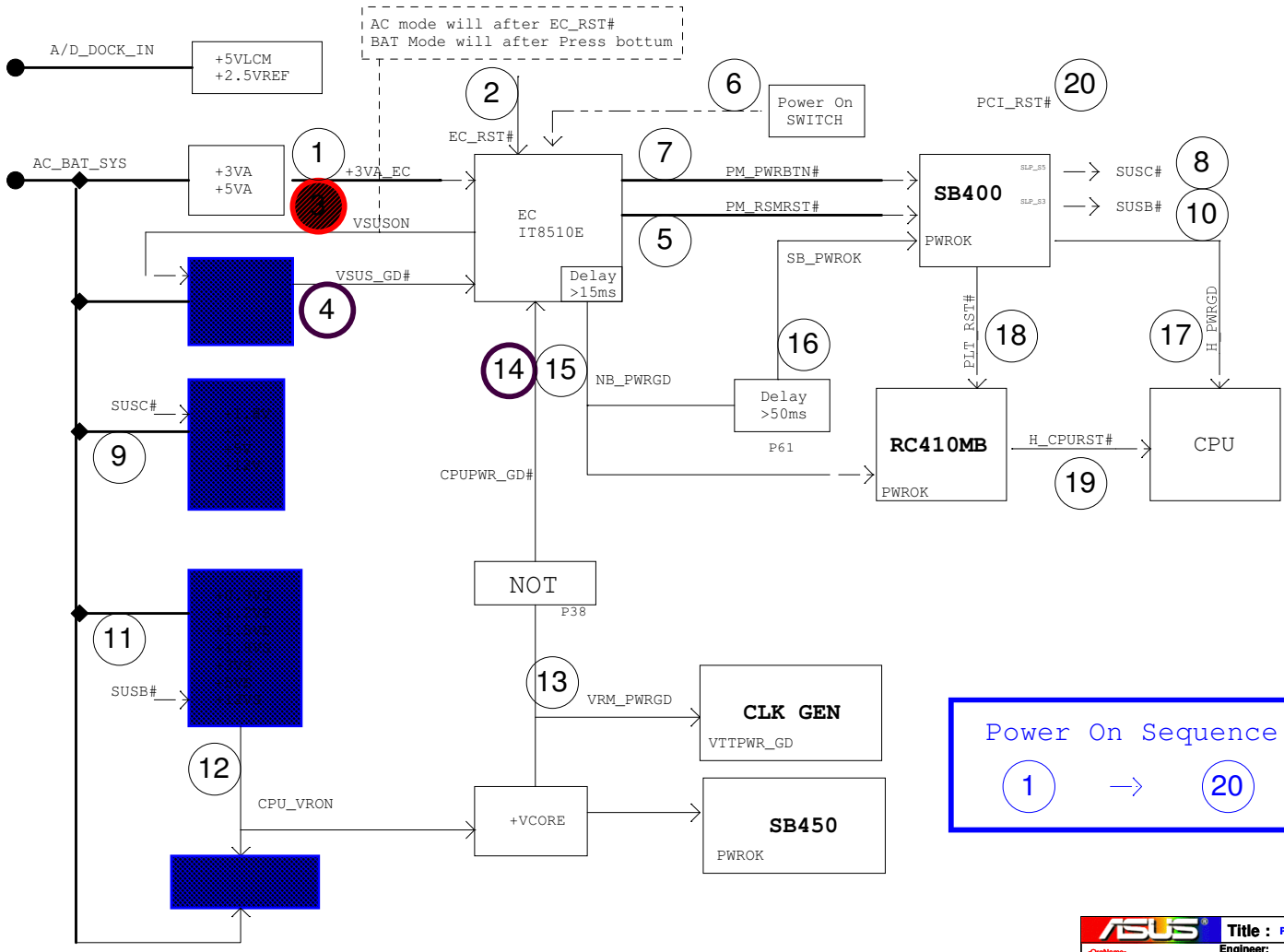
« Kennedy_Zhang »



PTH Hole

ASUS		Title : Hole	
<OrigName>	Project Name	Engineer:	Spring LI
Site	Custom		
	Z94Rp		
Date:	18.03.2018	Sheet:	33 of 45

« Kennedy_Zhang »



Power On Sequence
1 → 20

« Kennedy_Zhang »

ASUS		Title : Power Sequence	
<OrigName>	Project Name	Engineer:	Spring LI
Site	Customer		Rev
	Z94Rp		1.1
Date:	2018.11.13.2018	Sheet:	34 of 45

PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 LAN	AD16	0	E
CARD READER	AD17	1	B
CARDBUS	AD17	1	A

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	0101110x (5C)

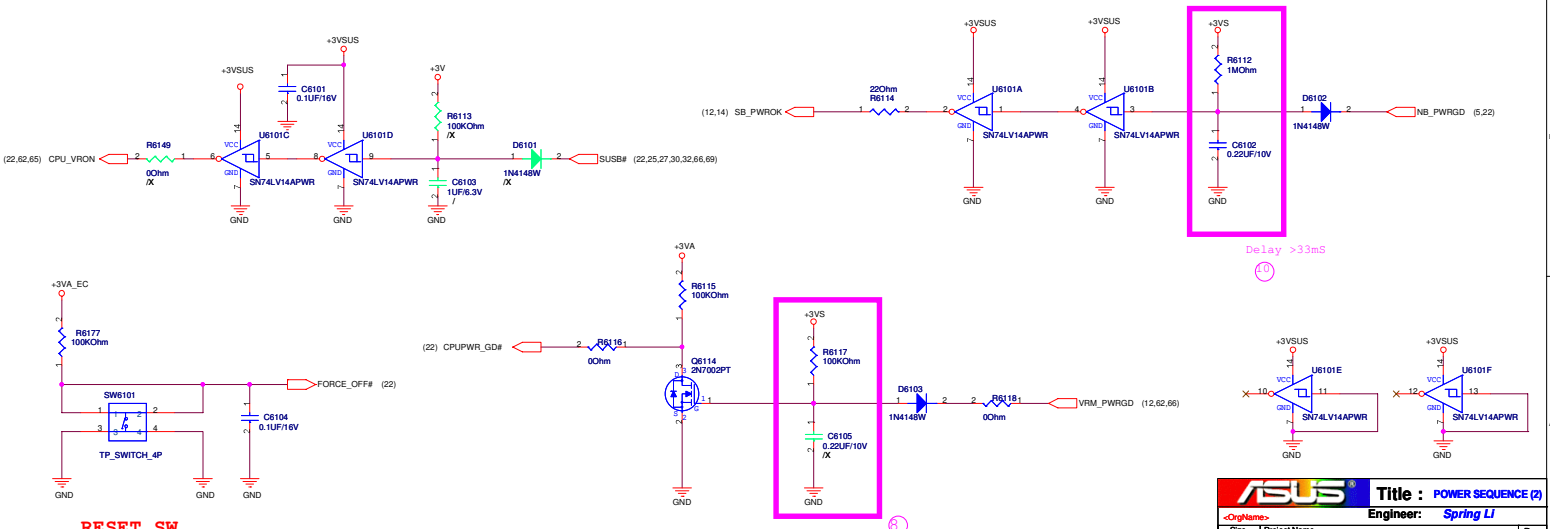
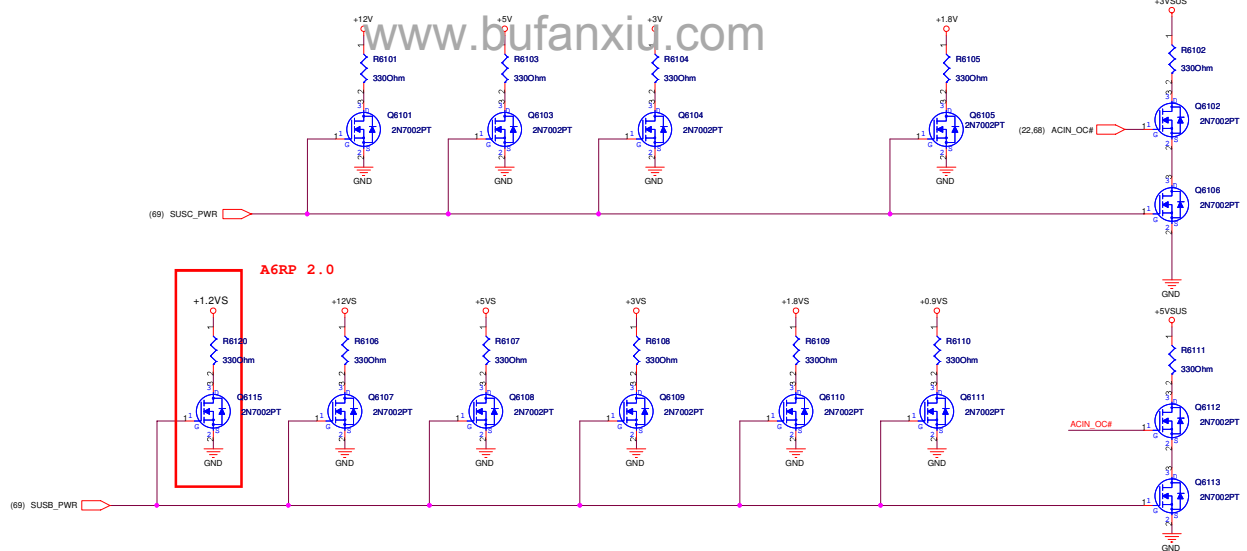
SB400 GPIO TABLE

GPIO	TYPE	POWER DOMAIN	FUNCTION
GPIO 0	I/OD	S0	
GPIO 1	I/O	S0	
GPIO 2	I/O	S0	SB_SPKR
GPIO 3	I/O	S0	
GPIO 4	I/O	S0	PCB_ID0
GPIO 5	I/O	S0	PCB_ID1
GPIO 6	I/OD	S0	PCB_ID2
GPIO 7	I/O	S0	VRM_PWRGD
GPIO 8	I/O	S0	CB_SD#
GPIO 9	I/O	S0	BACK_OFF#
GPIO 10	I/O	S5	SB_PM_THERM#
GPIO 11	I/O	S0	
GPIO 12	I/O	S0	
GPIO 13	I/O	S0	
GPIO 14	I/O	S0	
GPIO 31	I/O	S0	PCI_GNT#5
GPIO 32	I/O	S0	PCI_GNT#6
GPIO 33	I/O	S0	PCI_INTE#
GPIO 34	I/O	S0	PCI_INTF#
GPIO 35	I/O	S0	PCI_INTG#
GPIO 36	I/O	S0	PCI_INTH#
GPM 0	I	S5	
GPM 1	I	S5	
GPM 2	I/O	S5	
GPM 3	I	S5	
GPM 4	I	S5	
GPM 5	I	S5	
GPM 6	I/OD	S5	PWRLED_1HZ
GPM 7	I	S5	SYS_RESET#
GEVENT 0	I	S5	
GEVENT 1	I	S0	
GEVENT 2	I	S5	THRMTRIP#
GEVENT 3	I	S5	LPC_PME#
GEVENT 4	I	S5	PCI_PME#
GEVENT 5	I	S5	H_PROCHOT#
GEVENT 6	I	S5	
GEVENT 7	I	S5	
GEVENT 8			KB_SCI
EXTEVENT#0			EXT_SMI#
EXTEVENT#1			STO_SMI#

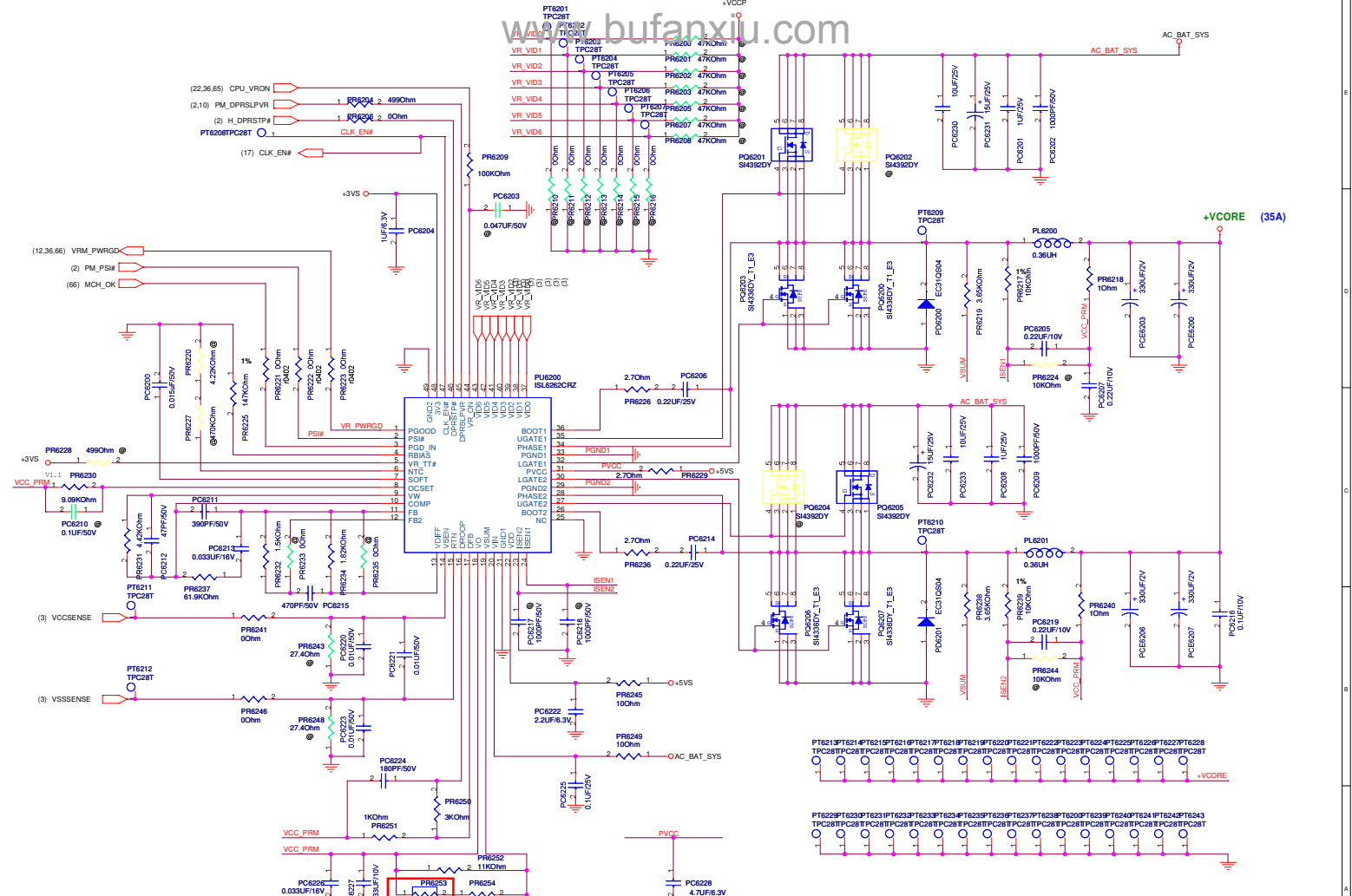
KBC GPIO	W1V	Note
P23(Pin 35)	CHG_FULL_OC	
P22(Pin 36)	BAT_LEARN	
P21(Pin 37)	LID_EC#	
P20(Pin 38)	KBCRSM	
P42(Pin 23)		
P43(Pin 22)	OP_SD#	
P44(Pin 21)	KB_CPURST	
P45(Pin 20)	KB_GATEA20	
P46(Pin 19)	KBCSCI#	
P47(Pin 18)	PM_CLKRUN#	
P50(Pin 17)	BAT_LLOW#_OC	
P51(Pin 16)	KID0	
P52(Pin 15)	KID1	
P53(Pin 14)		
P54(Pin 13)	BAT_SEL#	
P55(Pin 12)	BAT1_IN#_OC	
P56(Pin 11)		
P57(Pin 10)	INV_DA	
P67(Pin 74)		
P66(Pin 75)		
P65(Pin 76)	GAIN_AMP_K#	0 -> 0 W1V 1 -> NORMAL
P64(Pin 77)	ACIN_OC	
P63(Pin 78)	DISTP#	
P62(Pin 79)	MARATHON#	
P61(Pin 80)	INTERNET#	
P60(Pin 1)	EMAIL#	
P75(Pin 4)	KB_CLK	
P74(Pin 5)	MS_CLK	
P73(Pin 6)	TPAD_CLK	
P72(Pin 7)	KB_DAT	
P71(Pin 8)	MS_DAT	
P70(Pin 9)	TPAD_DAT	
P77(Pin 2)	SMC_BAT	
P76(Pin 3)	SMD_BAT	
P27(Pin 31)		
P26(Pin 32)	NUM_LED#	
P25(Pin 33)	CAP_LED#	
P24(Pin 34)	SET_PLTRSTNS#	
P40(Pin 27)	EXT_SMI	
P41(Pin 26)	EMAIL_LED#	

		Title : SYSTEM RESOURCE
Engineer: Spring Li		
Site: Custom	Project Name: Z94Rp	Rev: 1.1
Date: 08/24/2008	Sheet: 35	of 48

« Kennedy_Zhang »



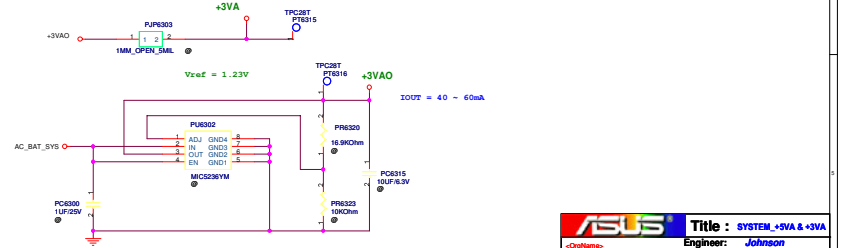
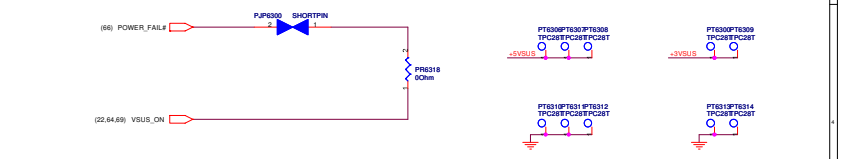
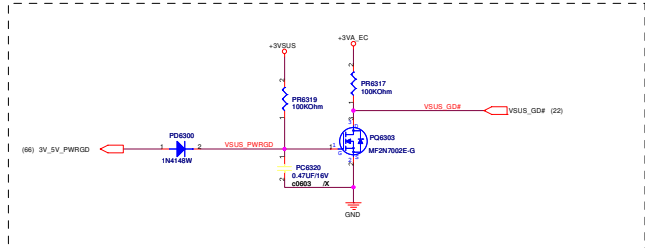
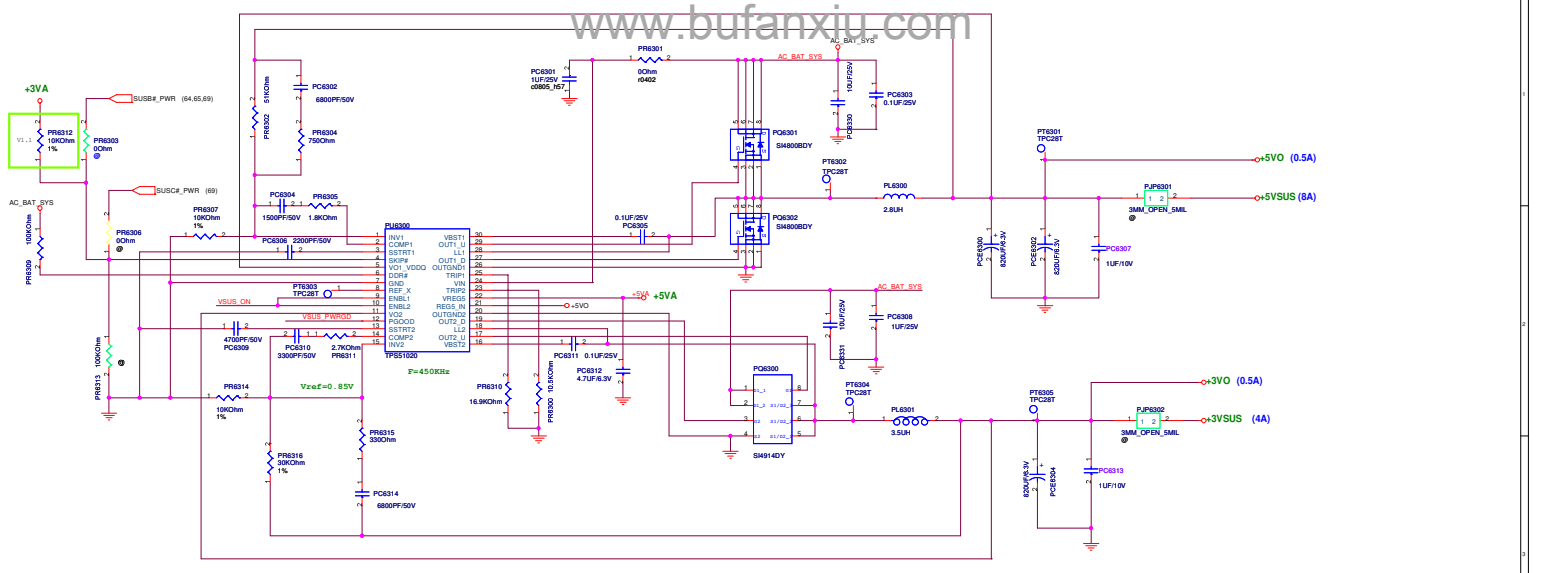
<< Kennedy_Zhang >>



Close to Phase 1 Inductor

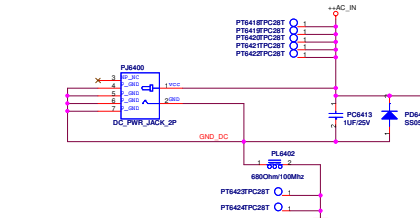
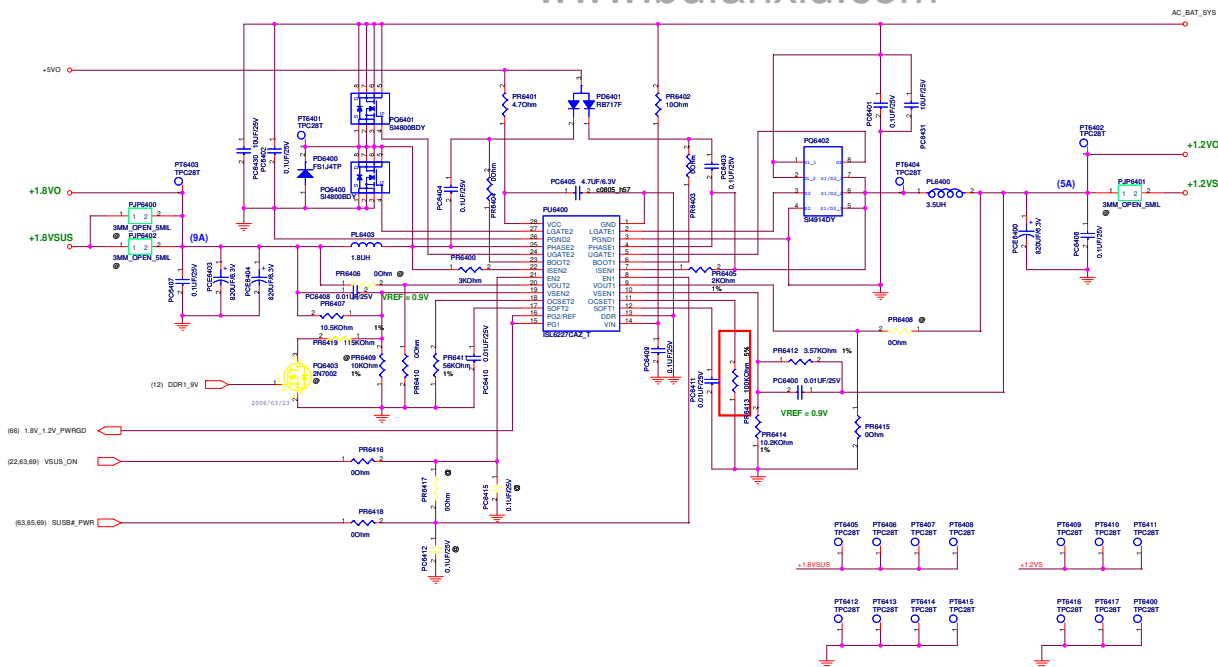
« Kennedy_Zhang »

		Title : POWER_VCORE
-<OrigName>		Engineer: Johnson
Site	Project Name	Rev
Custom	Z94Rp	1.1
Date: 2008.11.03.2008	Sheet	82 of 46



ASUS		Title : SYSTEM +5VA & +3VA	
Rev	Project Name	Engineer	Johnson
C	294Rp		
Date: 11/11/14 09:20:05	Sheet	61	of 65

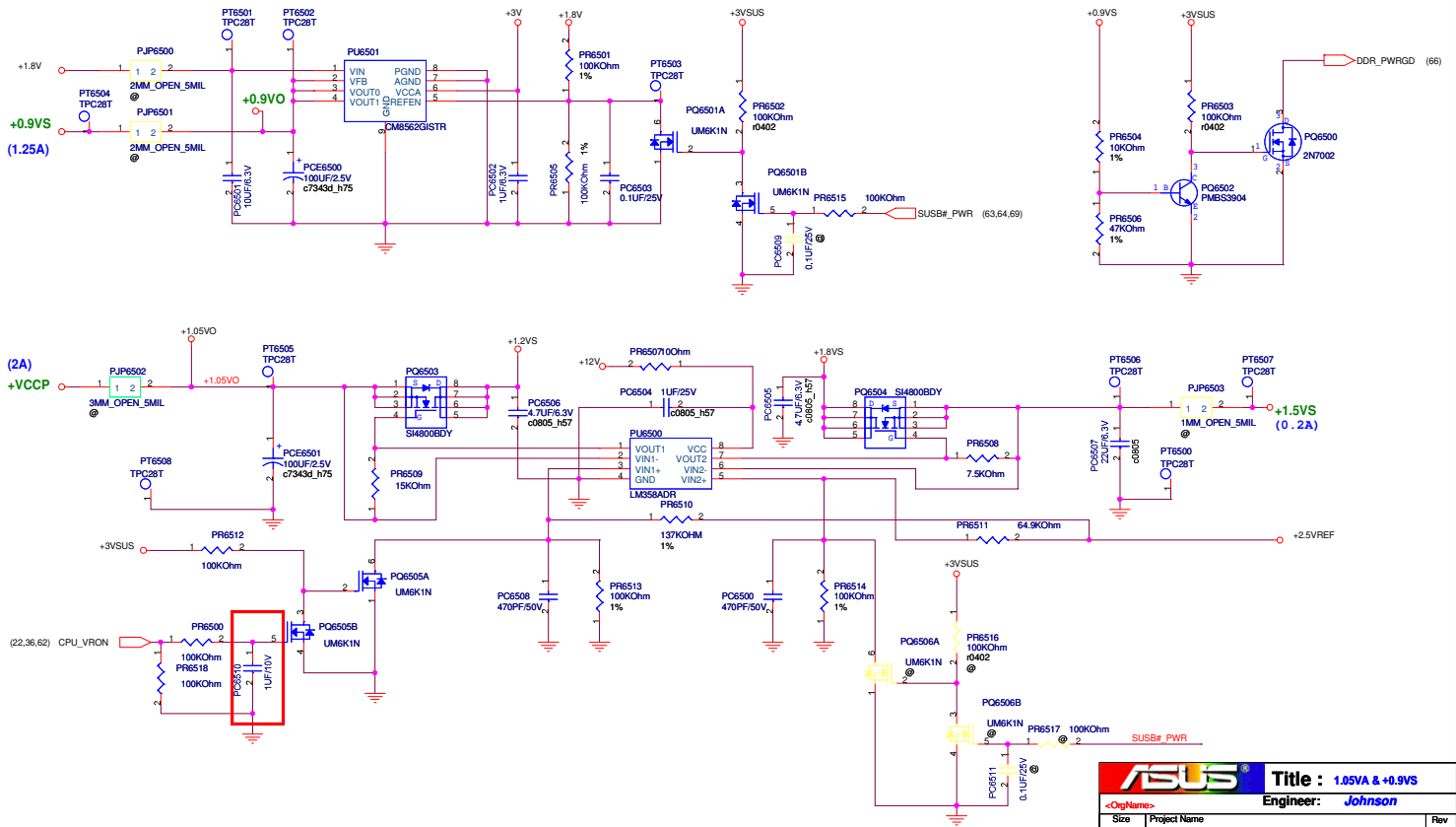
« Kennedy_Zhang »



Adaptor IN

		Title : 1.8V&1.2V	
-CircuitName-		Engineer: Johnson	
Ver	Project Name	Rev	
C	Z94Rp	1.1	
Date: 11/11/15 09:20:00	Sheet	54	of 65

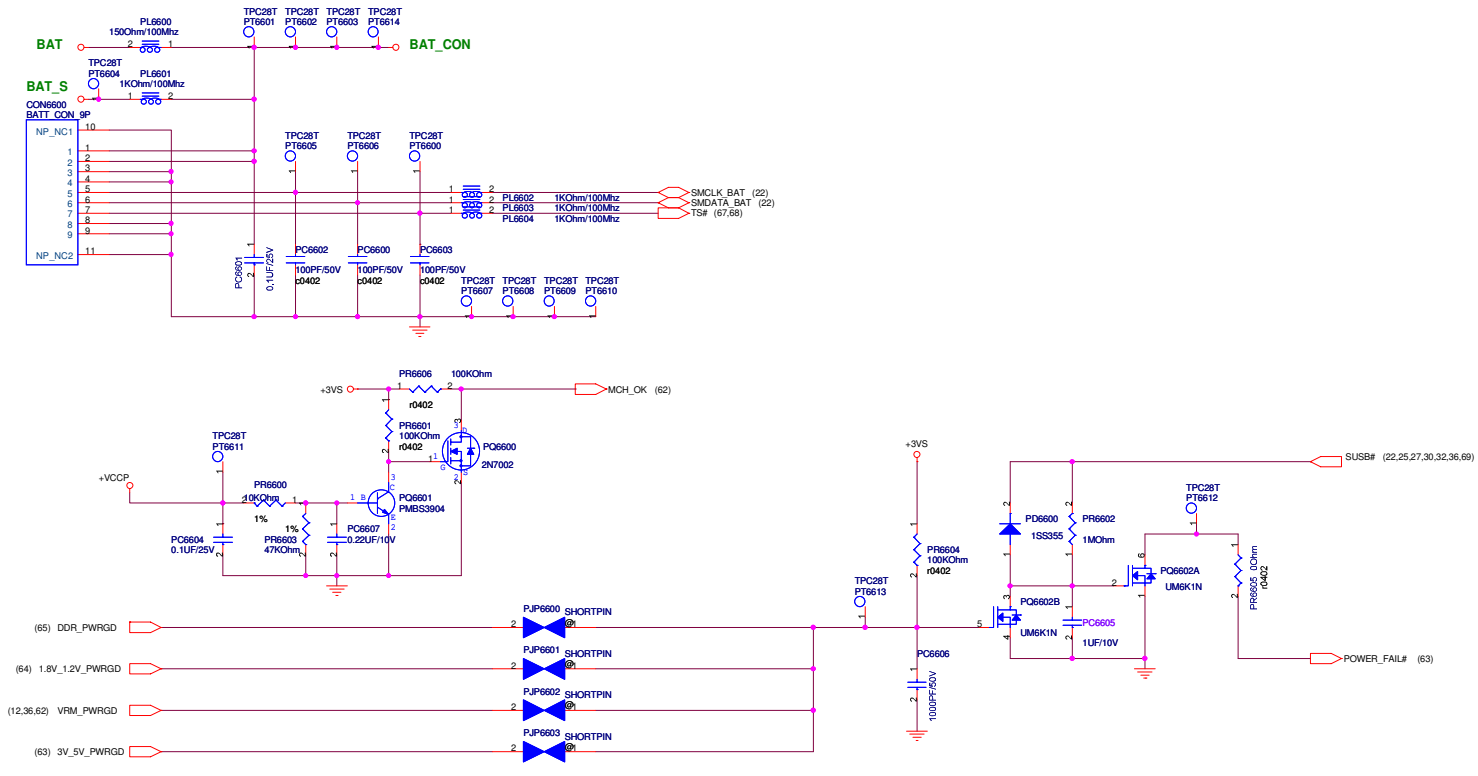
<< Kennedy_Zhang >>



ASUS Title : 1.05VA & +0.9VS
 Engineer: Johnson

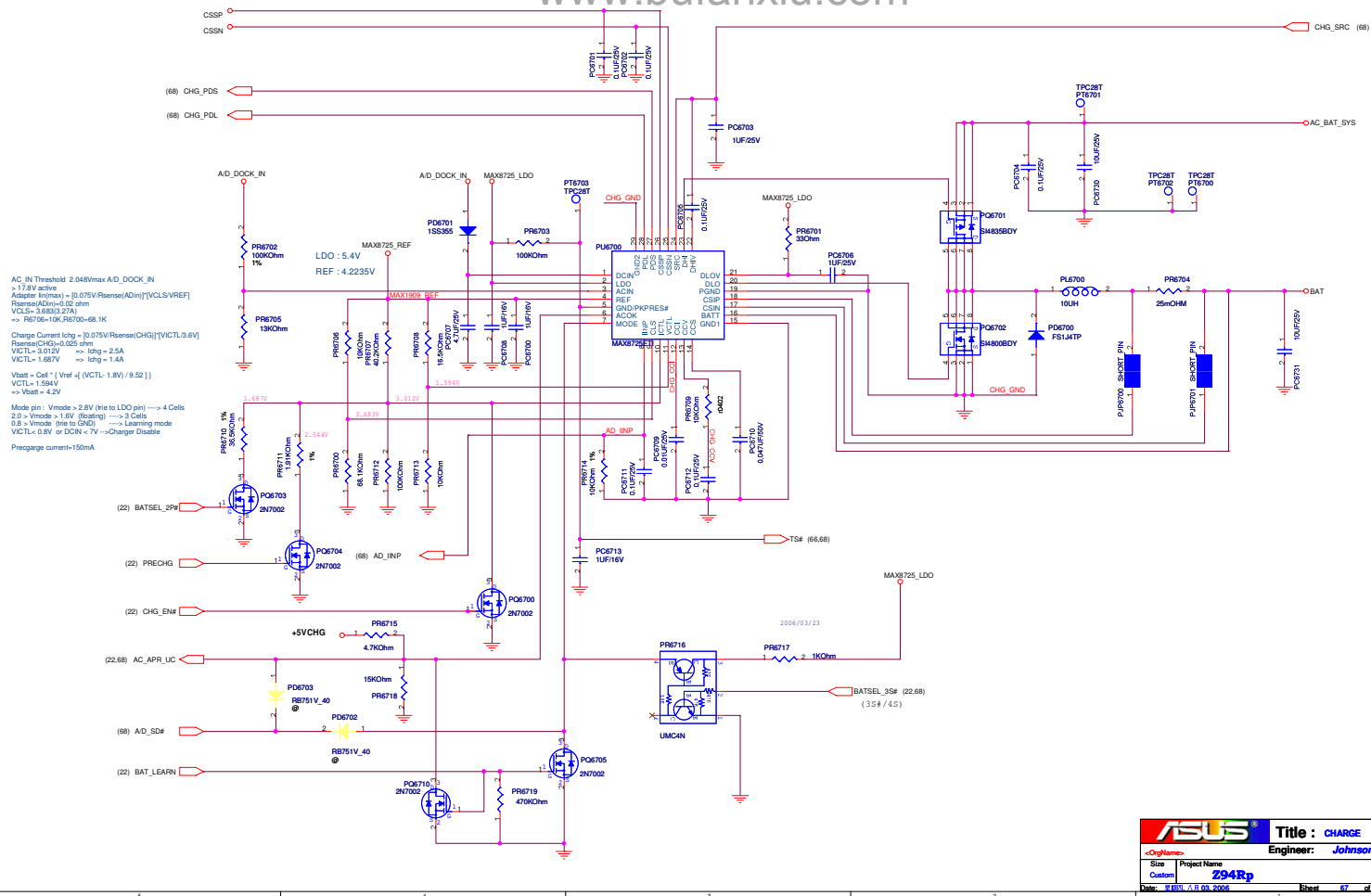
Size	Project Name	Rev
B	294Rp	1.1
Date: 8/13/03, 2005	Sheet	65 of 45

<< Kennedy_Zhang >>



ASUS		Title : BAT CON/PWOK	
-OrigName-		Engineer: Johnson	
Size	Project Name	Rev	
B	Z94Rp	1.1	
Date:	2006/11/03, 2006	Sheet	66 of 65

<< Kennedy_Zhang >>



AC_IN Threshold = 2.949Vmax A.D_DOCK_IN > 1.78V active
Adapter In(max) = 0.076V/Rsense(ADIN)(VCLS+VREF)
Rsense(ADIN)=0.02 ohm
VCLS= 0.8663-27A
=> R6705=10K,R6700=68.1K
Charge Current Ichg = [0.075V/Rsense(CHG)]*(VCTL-9.6V)
Rsense(CHG)=0.025 ohm
VCTL= 3.015V => Ichg = 2.5A
VCTL= 1.687V => Ichg = 1.4A
Vbat = Cell * Vref / (VCTL - 1.8V) / 9.52]
VCTL = 1.584V
=> Vbat = 4.2V
Mode pin : Vmode > 2.8V (tie to LDO pin) => 4 Cells
2.0 > Vmode > 1.8V (floating) => 3 Cells
0.8 > Vmode (tie to GND) => Learning mode
VCTL < 0.8V or DCIN < 7V => Charger Disable
Precharge current=150mA

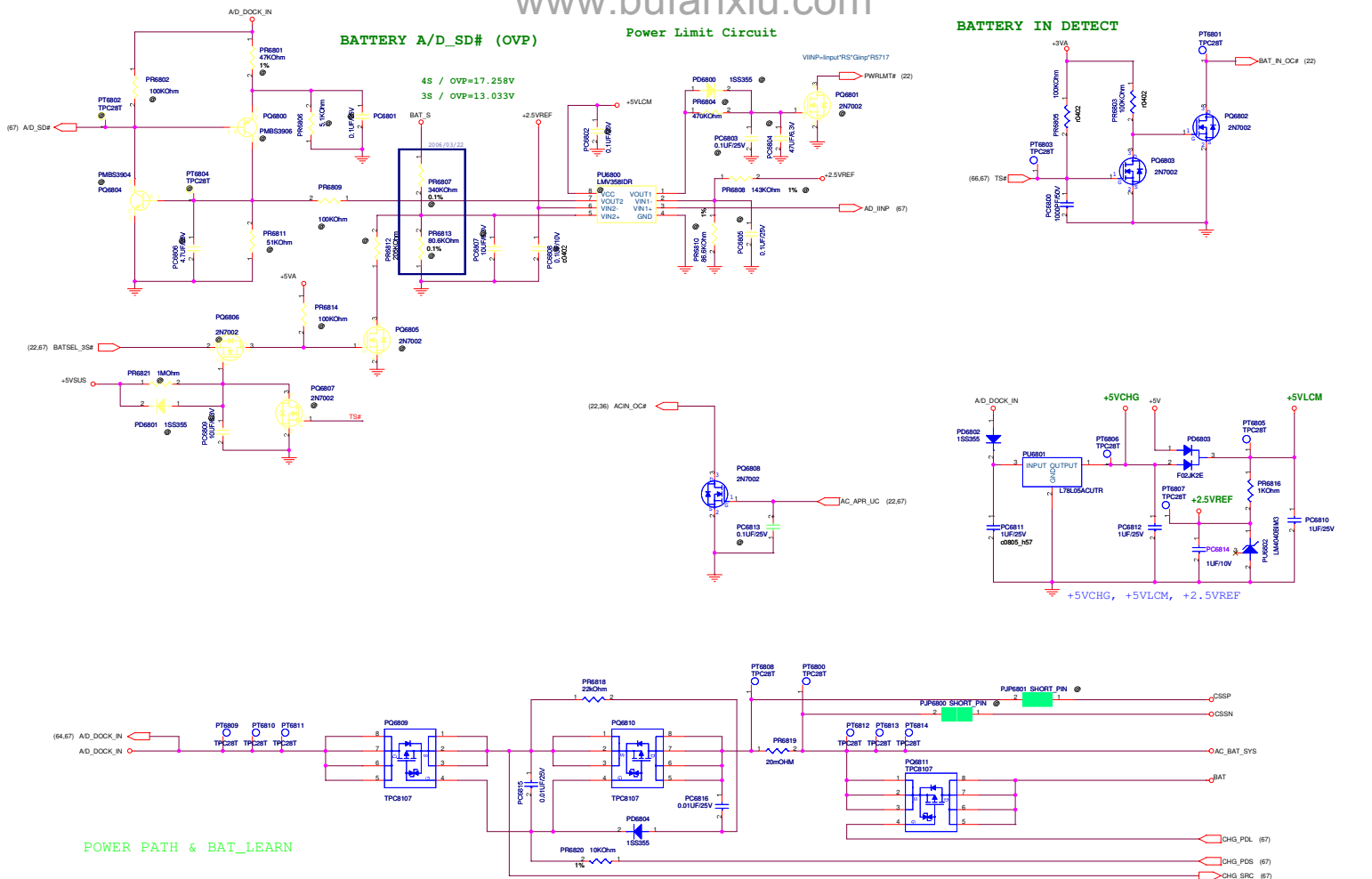
ASUS		Title : CHARGE	
<OrigName>		Engineer: Johnson	
Size	Project Name	Rev	
Custom	Z94Rp	1.1	
Date: 3/16/2006, 7:11:03 AM	Sheet	67 of 68	

<< Kennedy_Zhang >>

BATTERY A/D_SD# (OVP)

Power Limit Circuit

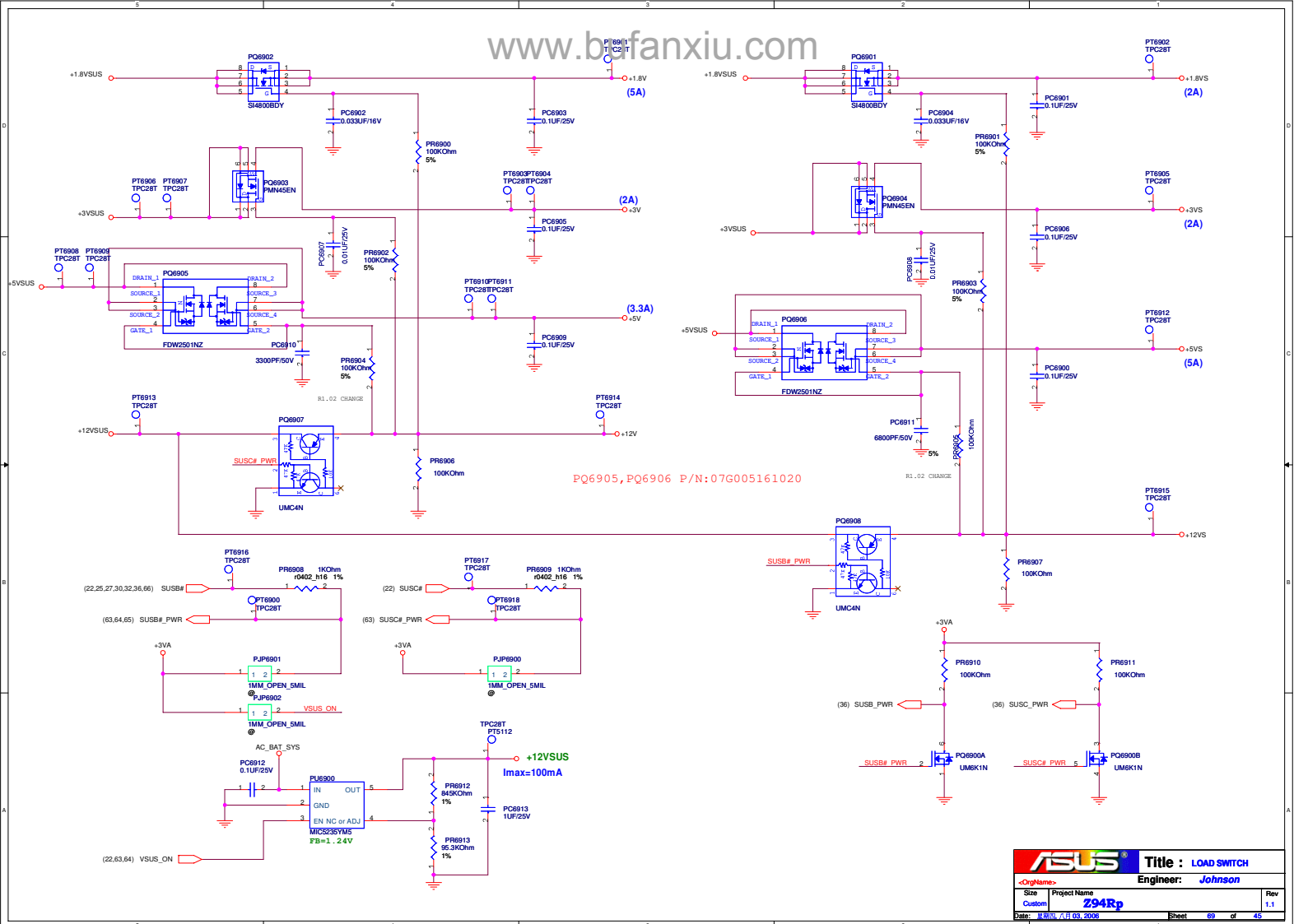
BATTERY IN DETECT



POWER PATH & BAT_LEARN

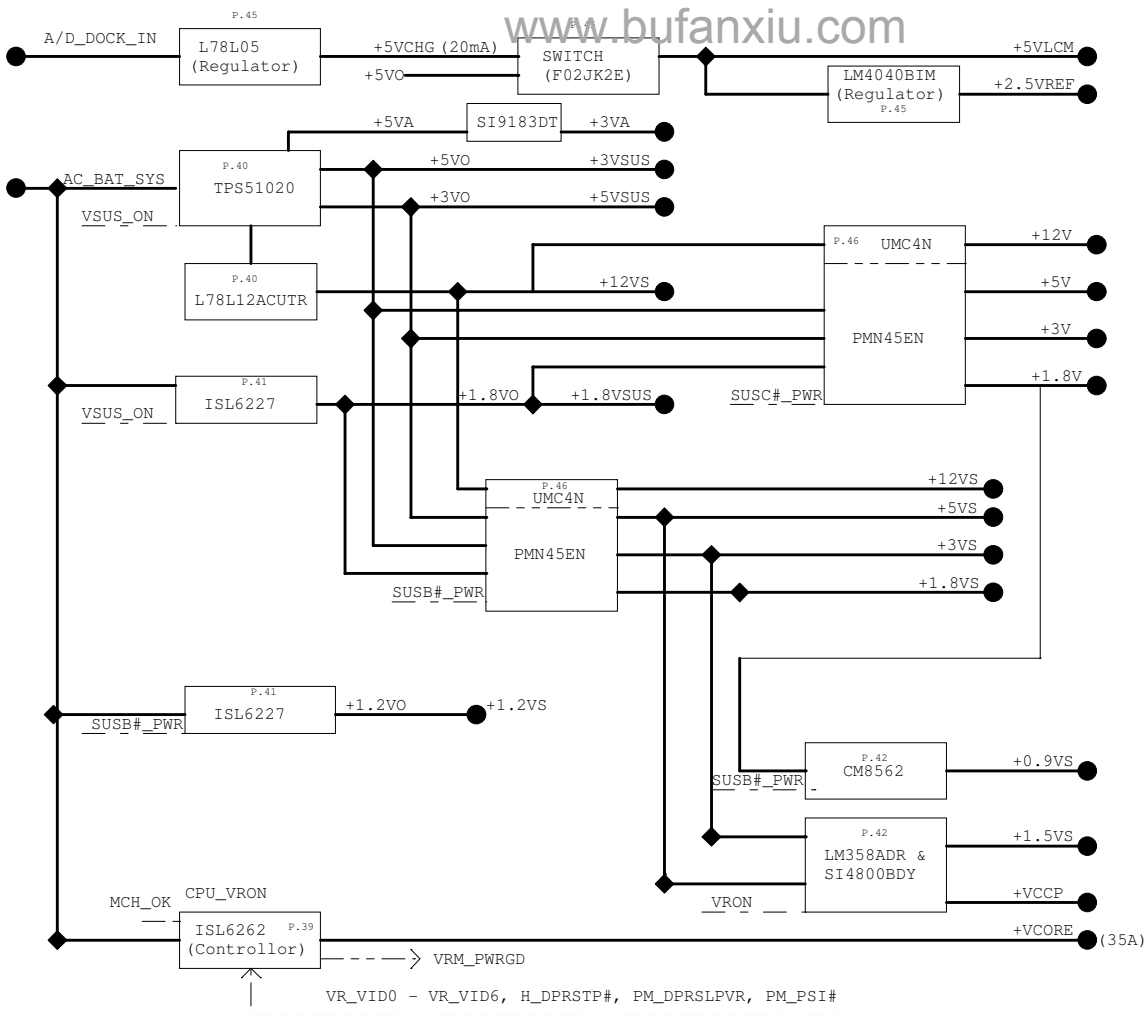
ASUS		Title : PROTECTIONSD#
Engineer:	Johnson	
Size	Project Name	Rev
Custom	Z94Rp	1.1
Date:	04/11/05, 2005	Sheet 08 of 45

<< Kennedy_Zhang >>



ASUS		Title : LOAD SWITCH	
Size	Project Name	Engineer:	Johnson
Custom	Z94Rp		
Date:	2008/03/03	Sheet	69 of 45

<< Kennedy_Zhang >>



« Kennedy_Zhang »

		Title : POWER BLOCK DIAGRAM	
Engineer:	Johnson		
Project Name:	Z94Rp		Rev: 1.1
Date:	2008.05.24	Sheet:	70 of 48